UNIT I
SMALL SIGNAL LOW FREQUENCY TRANSISTOR AMPLIFIER ANALYSIS
FET: Analysis of Common Source and Common Drain Amplifier circuits at low frequencies.

Introduction:
We have seen that V-I characteristics of an active device such as BJT are non-linear. The analysis of a non-linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation is possible only with small input signals. The term small signal amplifier refers to the use of signal that takes up a relatively small percentage of an amplifier's operational range. With small input signals the transistor can be replaced with small signal linear model. This model is also called small signal equivalent circuit.

We know that the reactance of the capacitance is inversely proportional to the frequency, \( Z_C = \frac{1}{2\pi fC} \). Thus for low frequencies the reactances of junction capacitances of the transistor are very high. Since these junction reactances appear in parallel with junctions, their effect is ignored at low frequencies and transistor analysis is further simplified.

An amplifier is used to increase the signal level; i.e. the amplifier is used to get a larger signal output from a small signal input. We will assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform, with frequency same as that of the input.

To make the transistor work as an amplifier, it is to be biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while base-collector junction to be reversed biased.
Let us consider the common emitter amplifier circuit using self bias or voltage divider bias as shown in the Fig. 5.1.

In the absence of input signal, only d.c. voltage are present in the circuit. This is known as zero-signal or no-signal condition or quiescent condition for the amplifier. The d.c. collector-emitter voltage, \( V_{CE} \), the d.c. collector current \( I_C \) and d.c. base current \( I_B \) is the quiescent operating point for the amplifier. On this d.c. quiescent operating point, we superimpose a.c. signal by application of a.c. sinusoidal voltage at the input. Due to this base current varies sinusoidally, as shown in Fig. 5.2.

Since the transistor is biased to operate in the active region, the output is linearly proportional to the input. The output current i.e. the collector current is \( \beta \) times larger than the input base current in common emitter configuration. Hence the collector current will also vary sinusoidally about its quiescent value, \( I_{CQ} \). The output voltage will also vary sinusoidally as shown in the Fig. 5.3 (a) and 5.3 (b).

Then variations in the collector current and the voltage between collector and emitter due to change in the base current are shown graphically with the help of load line in Fig. 5.3. The collector current varies above and below its Q point value in-phase with the base current, and the collector-to-emitter voltage varies above and below its Q point value 180° out-of-phase with the base voltage, as illustrated in Fig. 5.3 (c).

When one cycle of input is completed, one cycle of output will also be completed. This means the frequency of output sinusoidal is the same as the frequency of input sinusoid. Thus in the amplification process, frequency of the output signal does not change, only the magnitude of the output is larger than that of the input.
3. Emitter Bypass Capacitor \( C_E \)

An emitter bypass capacitor \( C_E \) is connected in parallel with the emitter resistance, \( R_E \) to provide a low reactance path to the amplified a.c. signal. If it is not inserted, the amplified a.c. signal passing through \( R_E \) will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. Output Coupling Capacitor \( C_2 \)

The coupling capacitor \( C_2 \) couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks d.c. and passes only a.c. part of the amplified signal.

**Need for \( C_1, C_2 \) and \( C_E \)**

We know that, the impedance of capacitor is given as

\[
X_C = \frac{1}{2\pi fC}
\]

5.2.1 Common Emitter Amplifier Circuit

Fig. 5.4 shows the practical circuit of common emitter transistor amplifier. It consists of different circuit component. The functions of these components are as follows:

1. **Biasing Circuit**

   The resistances \( R_1, R_2 \) and \( R_E \) forms the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.

2. **Input Capacitor \( C_1 \)**

   This capacitor couples the signal to the base of the transistor. It blocks any d.c. component present in the signal and passes only a.c. signal for amplification. Because of this biasing conditions are maintained constant.

   Thus, at signal frequencies all the capacitors have extremely small impedance and it can be treated as an a.c. short circuit. For bias/d.c. conditions of the transistor all the capacitors act as a d.c. open circuit. With this knowledge we will see the importance of \( C_1, C_2 \) and \( C_E \).

   Consider that the signal source is connected directly to the base of the transistor as shown in Fig. 5.5.

   Looking at the Fig. 5.5 we can immediately notice that source resistance \( R_s \) is in parallel with \( R_2 \). This will reduce the bias voltage at the transistor base and, consequently alter the collector current,
which is not desired. Similarly, by connecting $R_L$ directly, the d.c. levels of $V_C$ and $V_{CE}$ will change. To avoid this and maintain the stability of bias condition coupling capacitors are connected. As mentioned earlier, coupling capacitors act as open circuits to d.c., maintain stable biasing conditions even after connection of $R_i$ and $R_L$. Another advantage of connecting $C_1$ is that any d.c. component in the signal is opposed and only a.c. signal is routed to the transistor amplifier.

The emitter resistance $R_E$ is one of the component which provides bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor $C_E$ provides a low reactance path to the amplified a.c. signal increasing the output voltage swing.

For the proper operation of the circuit, polarities of the capacitors must be connected correctly. The curve bar which indicates negative terminal must always be connected at a d.c. voltage level lower than (or equal to) the d.c. level of the positive terminal (straight bar). For example, $C_1$ in Fig. 5.4 has its negative terminal at d.c. ground level, because it is

**Phase Reversal**

The phase relationship between the input and output voltages can be determined by considering the effect of a positive half cycle and negative half cycle separately. Consider the positive half cycle of input signal in which terminal A is positive w.r.t. B. Due to this, two voltages, a.c. and d.c. will be adding each other, increasing forward bias on base emitter junction. This increases base current. The collector current is $\beta$ times the base current, hence the collector current will also increase. This increases the voltage drop across $R_C$. Since $V_C = V_{CC} - I_C R_C$, the increase in $I_C$ results in a drop in collector voltage $V_C$, as $V_{CC}$ is constant. Thus, as $V_I$ increases in a positive direction, $V_C$ goes in a negative direction and we get negative half cycle of output voltage for positive half cycle at the input.

In the negative half cycle of input, in which terminal A becomes negative w.r.t. terminal B, the a.c. and d.c. voltages will oppose each other, reducing forward bias on base-emitter p-n junction. This reduces base current. Accordingly collector current and drop across $R_C$ both reduce, increasing the output voltage. Thus, we get positive half cycle at the output for negative half cycle at the input. Therefore, we can say that there is a phase shift of $180^\circ$ between input and output voltages for a common emitter amplifier.

### 5.2.2 Common Collector Amplifier Circuit

The Fig. 5.6 shows common collector circuit. The d.c. biasing is provided by $R_1$, $R_2$ and $R_E$. The load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied via to the base of the transistor, $V_B$ is increased and decreased as the signal goes positive and negative, respectively. Looking at Fig. 5.6 we can write that $V_E = V_B - V_{BE}$. Considering $V_{BE}$ fairly constant, we say that variation in the $V_B$ appears at emitter and emitter voltage $V_E$ will vary same as base voltage $V_B$. Since the emitter is output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. In other words, we can say that in common collector circuit emitter terminal follows the signal voltage applied to the base. Hence the common collector circuit is also known as an emitter follower.
5.2.3 Common Base Amplifier Circuit

Fig. 5.7 shows common base circuit. The signal source is coupled to the emitter of the transistor via $C_1$. The load resistance $R_L$ is coupled to the collector of the transistor via $C_2$.

The positive going pulse of input source increases the emitter voltage. As base voltage is constant, the forward bias of emitter base junction reduces. This reduces $I_b$, reducing $I_c$ and hence the drop across $R_c$. Since $V_o = V_{CC} - I_c R_C$, the reduction in $I_c$ results in an increase in $V_o$. Therefore, we can say that positive going input produces positive going output and similarly negative going input produces negative going output and there is no phase shift between input and output in a common base amplifier.

5.3 General Characteristics of Amplifier

The amplifier is a two port network having two input terminals and two output terminals, as shown in Fig. 5.8.

The signal to be amplified is applied to the input terminals and the load is connected to the output terminals. The amplified signal output is available across the load $R_L$. One of the input and output terminals are made generally common, i.e. a straight through connection. The signal to be amplified may be an a.c. or d.c. voltage. However we will assume the signal to be an a.c. signal so that the input and output voltages are sinusoidal, at some fixed or variable frequency.

The signal is a low level voltage such as obtained from a microphone, tape head, or a transducer. The output load may be a loudspeaker in an audio amplifier, a motor in a servo amplifier, a relay in control application, etc. In any case, the output of the amplifier is an enlarged version of the input. To amplify means to increase the amplitude of, raise the level of, or magnify input. Note that in the amplification process, the frequencies of the input and output signals are exactly identical. If not, there is "distortion" present in the amplifier. Then the signal is not faithfully reproduced at the output.

The amplifier is constructed using transistors. For their operation as an amplifier, transistors require proper d.c. biasing. The necessary d.c. voltage is provided by a battery (usually a dry battery) or a d.c. source resulting from a rectifier and filter combination. In this case, the amplifier operates from 230 V, 50 Hz a.c. mains supply. Very often, many amplifiers have the facility to operate from a.c mains or battery.
Referring to Fig. 5.8,

- $V_s$ : is the signal voltage,
- $R_s$ : is the internal resistance of the source,
- $V_i$ : is the actual input voltage to the amplifier,
- $I_i$ : is the input current to the amplifier,
- $V_2$ : is the output voltage across the load $R_L$,
- $I_2$ : is the output current flowing through the load $R_L$.

The ratio of $V_1$ to $I_1$ is called input resistance, $R_i$, of the amplifier. $R_i = \frac{V_1}{I_1}$

$V_2$ is the output voltage across the load $R_L$, and $I_2$ is the output current flowing through the load $R_L$. $R_o$ is the output (or internal) resistance of the amplifier.

The ratio of output current to input current is called current gain, $A_I$, of the amplifier.

Current gain, $A_I = \frac{I_2}{I_1}$.

The ratio of output voltage to input voltage is known as voltage gain, $A_V = \frac{V_2}{V_1}$.

The ratio of signal power delivered to the load to the signal power at the input of the amplifier is the power gain.

Power gain, $A_p = \frac{P_2}{P_1} = \frac{V_2 I_2}{V_1 I_1}$.

$\therefore A_p = \frac{V_2}{V_1} \times \frac{I_2}{I_1} = A_V A_I$

An amplifier may or may not exhibit both a voltage and a current gain, but in general will show a power gain. However, whether voltage or power gain is more important depends upon the application. The amplifier, in which voltage gain is more important than the power gain, is called a voltage amplifier, while in which power gain is more important than voltage gain is known as power amplifier.

To do the analysis of amplifier circuit we have to replace it by its equivalent circuit. In the next section we see the hybrid model which simplifies analysis of the amplifier circuit.

Small Signal Low Frequency h-parameter model:

**2.10 Hybrid Model**

Let us consider transistor amplifier as a black box as shown in the Fig. 2.41.

![Fig. 2.41 Transistor amplifier](image)

Here, $I_i$ : is the input current to the amplifier.

$V_i$ : is the input voltage to the amplifier.

$I_o$ : is the output current of the amplifier and

$V_o$ : is the output voltage of the amplifier.
As we know transistor is a current operated device, input current is an independent variable. The input current, \( I_i \) and output voltage \( V_o \) devices the input voltage \( V_i \) as well as the output current \( I_o \). Hence input voltage \( V_i \) and output current \( I_o \) are the dependent variables, whereas input current \( I_i \) and output voltage \( V_o \) are independent variables. Thus we can write

\[
V_i = f_1 (I_i, V_o) \quad \text{... (1)}
\]

\[
I_o = f_2 (I_i, V_o) \quad \text{... (2)}
\]

This can be written in the equation form as follows

\[
V_i = h_{11} I_i + h_{12} V_o \quad \text{... (3)}
\]

\[
I_o = h_{21} I_i + h_{22} V_o \quad \text{... (4)}
\]

The above equations can also be written using alphabetic notations,

\[
V_i = h_i I_i + h_r V_o \quad \text{... (5)}
\]

\[
I_o = h_f I_i + h_o V_o \quad \text{... (6)}
\]

**Definitions of \( h \)-parameter**

The parameters in the above equation are defined as follows:

\[
h_{11} = \left. \frac{V_i}{I_i} \right|_{V_o=0} = \text{Input resistance with output short-circuited, in ohms.}
\]

\[
h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i=0} = \text{Fraction of output voltage at input with input open circuited.}
\]

This parameter is ratio of similar quantities, hence unitless.

\[
h_{21} = \left. \frac{I_o}{I_i} \right|_{V_o=0} = \text{Forward current transfer ratio or current gain with output short circuited.}
\]

This parameter is a ratio of similar quantities, hence unitless.

\[
h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i=0} = \text{Output admittance with input open-circuited, in mhos.}
\]

From the above discussion we can say that, these four parameters are not same. They have different units. In other words, they are mixture of different units and hence referred to as hybrid parameters. As we use small letter for a.c. analysis, these are commonly known as \( h \)-parameters. The standard notations can be given as

\[
i = 11 = \text{Input} \quad o = 22 = \text{Output}
\]

\[
f = 21 = \text{Forward transfer} \quad r = 12 = \text{Reverse transfer}
\]

Thus we can write \( h \)-parameters as follows.

**a) With output short circuited :**

\[h_{11} = h_i : \text{Input resistance}\]

\[h_{21} = h_f : \text{Short circuit current gain}\]

**b) With input open circuited :**

\[h_{12} = h_r : \text{Reverse voltage transfer ratio}\]

\[h_{22} = h_o : \text{Output admittance}\]
h-parameter equivalent circuit for transistor

In order to analyze transistorized amplifier circuit and calculate its input impedance, output impedance, current gain and voltage gain, it is necessary to replace transistor circuit with its equivalent. The equivalent circuit can be drawn with the help of two equations, as shown in Fig. 2.42.

\[ V_i = h_{i} I_i + h_r V_o \]
\[ I_o = h_f I_i + h_v V_o \]

Many transistor models have been proposed, each one having its advantages and disadvantages. The transistor model used in this text is in terms of h-parameters.

Benefits of h-parameters

1. Real numbers at audio frequencies.
2. Easy to measure.
3. Can be obtained from the transistor static characteristic curves.
4. Convenient to use in circuit analysis and design.
5. Most of the transistor manufacturers specify the h-parameters.

h-parameter equivalent circuit for CE configuration

To see how we can derive a hybrid model for a transistor, let us consider the common emitter configuration shown in Fig. 2.43. The variables \( I_b, I_c, V_b \) and \( V_c \) represent total instantaneous currents and voltages.

\[ I_b = \text{Input current} \]
\[ I_c = \text{Output current} \]
\[ V_{be} = \text{Input voltage} \]
\[ V_{ce} = \text{Output voltage} \]

Fig. 2.44 shows the h-parameter equivalent circuit for the common emitter configuration.
From the h-parameter equivalent circuit of the common emitter configuration we can write,

\[ V_{be} = h_{ie} I_b + h_{re} V_{ce} \]  \hspace{2cm} \ldots (7)

\[ I_c = h_{fe} I_b + h_{oe} V_{ce} \]  \hspace{2cm} \ldots (8)

where,

\[ h_{ie} = \left. \frac{\Delta V_{BE}}{\Delta I_b} \right|_{V_{CE} \text{ constant}} \]  \hspace{2cm} \ldots (9)

\[ h_{re} = \left. \frac{\Delta V_{BE}}{\Delta V_{CE} I_b} \right|_{I_b \text{ constant}} \]  \hspace{2cm} \ldots (10)

\[ h_{fe} = \left. \frac{\Delta I_C}{\Delta I_b} \right|_{V_{CE} \text{ constant}} \]  \hspace{2cm} \ldots (11)

\[ h_{oe} = \left. \frac{\Delta I_C}{\Delta V_C I_b} \right|_{I_b \text{ constant}} \]  \hspace{2cm} \ldots (12)

The quantities \( \Delta V_{BE} \) (\( V_{be} \)), \( \Delta V_{CE} \) (\( V_{ce} \)), \( \Delta I_B \) (\( I_b \)) and \( \Delta I_C \) (\( I_c \)) represent the small change in base and collector voltages and currents.

**h-parameters for all three configurations**

As mentioned earlier, transistor can be represented as a two port network by making any one terminal common between input and output. Since there are three possible configurations in which a transistor can be used, there is a change in terminal voltage and current for different transistor configurations. For different configurations the relation between input parameters and output parameters also differs. Therefore, one needs to define different set of h-parameters for different configurations. To designate the type of configuration another subscript is added to the h-parameters.

For example:

\[ h_{ie} = h_{1ie} = \text{Input resistance in common emitter configuration.} \]

\[ h_{fe} = h_{21b} = \text{Short-circuit current gain in common base configuration.} \]

The Table 2.3 summarizes the h-parameters for all the three configurations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CB</th>
<th>CE</th>
<th>CC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input resistance</td>
<td>( h_{bb} )</td>
<td>( h_{ie} )</td>
<td>( h_{ic} )</td>
</tr>
<tr>
<td>Reverse voltage gain</td>
<td>( h_{rf} )</td>
<td>( h_{re} )</td>
<td>( h_{rc} )</td>
</tr>
<tr>
<td>Forward transfer current gain</td>
<td>( h_{fb} )</td>
<td>( h_{fc} )</td>
<td>( h_{fc} )</td>
</tr>
<tr>
<td>Output admittance</td>
<td>( h_{ob} )</td>
<td>( h_{oe} )</td>
<td>( h_{oe} )</td>
</tr>
</tbody>
</table>

**Table 2.3**
The basic circuit of hybrid model is same for all the three configurations, only parameters are different. The Fig. 2.45 shows the transistor configurations and their hybrid models.

The circuits and equations in Fig. 2.45 are valid for either an n-p-n or p-n-p transistor and are independent of the type of load or method of biasing.

![Transistor configurations and their hybrid models](image)

Fig. 2.45 Transistor configurations and their hybrid models

### 2.10.1 Determination of h-Parameters from Characteristics

Let us consider common emitter configuration. Its functional relationship can be defined from equations (1) and (2) from section 2.10 as

\[
V_{be} = f_1 (I_b, V_{ce}) \quad \ldots \quad (1)
\]

\[
I_c = f_2 (I_b, V_{ce}) \quad \ldots \quad (2)
\]

![Typical input characteristic curves for the common emitter transistor](image)

Fig. 2.46 Typical input characteristic curves for the common emitter transistor

We have already seen the relationship between input and output voltages and currents from the characteristic curves discussed in the chapter 5. The input characteristic curves give the relationship between input voltage \( V_{BE} \) and the input current \( I_B \) for different values of output voltage \( V_{CE} \).

Fig. 2.46 shows typical input characteristic curves for the common emitter transistor configuration.
2.10.1.1 Determination of $h_{ie}$ and $h_{re}$ from Input Characteristic Curves

Parameter $h_{ie}$: From equation 9 from section 2.10 we have,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE\text{constant}}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}} \quad \ldots (3)$$

The parameter $h_{ie}$ can be obtained as the change in the base voltage, $V_{BE2} - V_{BE1}$, divided by the change in the base current, $I_{B2} - I_{B1}$, for a constant collector voltage at the quiescent point, $Q$.

The slope of the line EF, drawn tangent to the input characteristic curve at the point $Q$ gives $h_{ie}$.

Parameter $h_{re}$: From equation (10) of section 2.10 we have,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \bigg|_{I_{B\text{constant}}} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}} \quad \ldots (4)$$

A horizontal line on the input characteristics of Fig. 2.46 represents constant base current. The parameter $h_{re}$ can be obtained as the change in base voltage, $V_{BE2} - V_{BE1}$, divided by the change in collector voltage, $V_{CE2} - V_{CE1}$, for a constant base current $I_B$, at the quiescent point $Q$.

The output characteristic curves give the relationship between output current $I_C$ and output voltage $V_{CE}$ for different values of input current $I_B$. Fig. 2.47 shows typical output characteristic curves for the common emitter transistor configuration.

![Fig. 2.47 Typical output characteristic curves for common emitter configuration](image)

2.10.1.2 Determination of $h_{fe}$ and $h_{oe}$ from Output Characteristic Curves

Parameter $h_{fe}$:

From equation (11) of section 2.10 we have,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE\text{constant}}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} \quad \ldots (5)$$

It is the ratio of change in collector current $I_C$ taken around the quiescent point $Q$ to the corresponding change in the base current $I_B$, for constant value of output voltage $V_{CE}$ at the $Q$-point.

Parameter $h_{oe}$:

From equation (12) of section 2.10 we have,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_C} \bigg|_{I_{B\text{constant}}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}} \quad \ldots (6)$$
The parameter $h_{oc}$ can be obtained as the change in the collector current, $I_{C2} - I_{C1}$, divided by the change in the collector voltage, $V_{CE2} - V_{CE1}$, for a constant base current at the quiescent point Q. The slope of the line AB, drawn tangent to the output characteristic curve at the point Q gives $h_{oc}$. By using similar procedure it is possible to obtain $h$-parameters for common base and common collector configurations from the appropriate input and output characteristic curves.

From the above discussion it can be noticed that $h$-parameters are always calculated at quiescent operating point of the amplifier.

### 2.10.2 Midband Analysis of Single Stage Characteristics

The Fig. 2.48 shows basic amplifier circuit. From the Fig. 2.48 we can notice that to form a transistor amplifier only it is necessary to connect an external load and signal source, along with proper biasing. Fig. 2.48 represents a transistor in any one of the three possible configurations.

![Fig. 2.48 Basic transistor amplifier](image)

We can replace transistor circuit shown in Fig. 2.48 with its small signal hybrid model as shown in Fig. 2.49.

![Fig. 2.49 Transistor amplifier in its h-parameter model](image)

Let us analyze hybrid model to find the current gain, the input resistance, the voltage gain, and the output resistance.

**Current Gain ($A_i$):**

For transistor amplifier $A_i$ is defined as the ratio of output to input currents. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \quad \text{... (1)}$$

Here $I_L$ and $I_2$ are equal in magnitude but opposite in sign, i.e. $I_L = -I_2$

From the circuit of Fig. 2.51 We have,

$$I_2 = h_f I_1 + h_o V_2 \quad \text{... (2)}$$

Substituting $V_2 = -I_2 R_L$ in the equation we obtain
Substituting $V_2 = -I_2 R_L$ in the equation we obtain

$$I_2 = h_f I_1 + h_o ( -I_2 R_L )$$

\[
\therefore I_2 + h_o I_2 R_L = h_f I_1 \\
\therefore (1 + h_o R_L) I_2 = h_f I_1 \\
\therefore \frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L} \\
\therefore A_i = -\frac{I_2}{I_1} = -\frac{h_f}{1 + h_o R_L} \quad \ldots (3)
\]

**Current Gain ($A_{1S}$)**

It is the current gain taking into account the source resistance, $R_S$ if the model is driven by the current source instead of voltage source. It is given by

$$A_{1S} = \frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s} \quad \ldots (4)$$

$$= A_i \cdot \frac{I_1}{I_s}$$

*Fig. 2.50*

Looking at Fig. 2.50 (b) and using current divider equation we get

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

\[
\therefore \frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s} \\
\text{and hence} \quad A_{1S} = \frac{A_i \cdot R_s}{Z_i + R_s} \quad \ldots (5)
\]

**Input Impedance ($Z_i$)**

As shown in the Fig. 2.48, $R_i$ is the input resistance looking into the amplifier input terminals (1, 1'). It is given by,

$$R_i = \frac{V_1}{I_1} \quad \ldots (6)$$

From the input circuit of Fig. 2.51, we have

$$V_1 = h_i I_1 + h_r V_2 \quad \ldots (7)$$

Hence

$$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$
\[ Z_i = h_i + h_r \frac{V_2}{I_1} \]  \hspace{1cm} ... (8)

Substituting \[ V_2 = -I_2 R_L = A_i I_1 R_L \]  \hspace{1cm} ... (9)

In the above equation we get,
\[ Z_i = h_i + h_r A_i \frac{I_1 R_L}{I_1} = h_i + h_r A_i R_L \]  \hspace{1cm} ... (10)

Substituting \[ A_i = -\frac{h_f}{1 + h_o R_L} \]

We get, \[ Z_i = h_i - h_r h_f \frac{R_L}{1 + h_o R_L} \]  \hspace{1cm} ... (11)

Dividing numerator and denominator by \( R_L \) we get
\[ Z_i = h_i - h_r \frac{h_f}{1/R_L + h_o} \]

\[ \therefore \quad Z_i = h_i - h_r \frac{h_f}{\gamma_L + h_o} \quad \text{where} \quad \gamma_L = \frac{1}{R_L} \]  \hspace{1cm} ... (12)

From this equation we can note that input impedance is a function of the load impedance.

Voltage Gain (\( A_v \)):

It is the ratio of output voltage \( V_2 \) to the input voltage \( V_1 \). It is given by
\[ A_v = \frac{V_2}{V_1} \]  \hspace{1cm} ... (13)

From equation (9) we have,
\[ A_v = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i} \]  \hspace{1cm} ... (14)

Since, \[ \frac{I_1}{V_1} = \frac{1}{Z_i} \]

Voltage Gain (\( A_{vs} \)):

It is voltage gain including the source. It is given by,
\[ A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} \]  \hspace{1cm} ... (15)

\[ \therefore \quad A_{vs} = A_v \times \frac{V_1}{V_s} \]  \hspace{1cm} ... (16)

Looking at Fig. 2.51 and applying potential divider theorem we can write,
\[ V_1 = \frac{Z_i}{R_s + Z_i} V_s \]

\[ \therefore \quad \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i} \]
Substituting value of $\frac{V_1}{V_s}$ in equation (16) We get,

$$A_{VS} = A_v \cdot \frac{Z_i}{R_s + Z_i}$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \therefore A_v = \frac{A_i R_L}{Z_i}$$  \hspace{1cm} \ldots \text{(17)}$$

**Output Admittance $Y_o$:**

It is the ratio of output current $I_2$ to the output voltage $V_2$. It is given by,

$$Y_o = \frac{I_2}{V_2} \quad \text{with} \quad V_s = 0$$  \hspace{1cm} \ldots \text{(19)}$$

From equation (2), we have,

$$I_2 = h_f I_1 + h_o V_2$$

Dividing above equation by $V_2$ we get,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$\therefore Y_o = h_f \frac{I_1}{V_2} + h_o$$  \hspace{1cm} \ldots \text{(20)}$$

From Fig. 2.49, with $V_s = 0$ we can write,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$  \hspace{1cm} \ldots \text{(21)}$$

$$\therefore (R_s + h_i) I_1 = -h_r V_2$$

$$\therefore \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$  \hspace{1cm} \ldots \text{(22)}$$

Substituting value of $\frac{I_1}{V_2}$ from equation (22) in equation (20), we obtain,

$$Y_o = h_o - \frac{h_r h_f}{h_i + R_s}$$ \hspace{1cm} \ldots \text{(23)}$$

From this equation we can note that output admittance is a function of the source resistance.

**Power Gain ($A_P$):** It is the ratio of average power delivered to the load $R_L$, to the input power. Output power is given as

$$P_2 = V_2 I_L = -V_2 I_2$$ \hspace{1cm} \ldots \text{(24)}$$

Since the input power is $P_1 = V_1 I_1$ the operating power gain $A_P$ of the transistor is defined as

$$A_P = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_v A_i = A_i^2 \frac{R_L}{Z_i} \quad \therefore A_v = \frac{A_i R_L}{Z_i}$$ \hspace{1cm} \ldots \text{(25)}$$

**Relation between $A_{VS}$ and $A_{IS}$:**

From equations (18) and equation (5) we have

$$A_{VS} = \frac{A_i R_L}{Z_i + R_s}$$

and

$$A_{IS} = \frac{A_i R_s}{Z_i + R_s}$$

Taking ratio of above two equations we get,

$$\frac{A_{VS}}{A_{IS}} = \frac{R_L}{R_s}$$

$$\therefore A_{VS} = A_{IS} \frac{R_L}{R_s}$$ \hspace{1cm} \ldots \text{(26)}$$
Table 2.4 summarizes small-signal analysis of a transistor amplifier.

\[ A_i = - \frac{h_f}{1 + h_o R_L} \]
\[ A_{a} = \frac{A_i R_s}{Z_i + R_s} \]
\[ Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L} \]
\[ A_v = \frac{A_i R_L}{Z_i} \]
\[ A_{v_b} = \frac{A \cdot R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{a} R_L}{R_s} \]
\[ Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o} \]
\[ A_p = A_v A_i = A_i^2 \frac{R_L}{Z_i} \]

**Table 2.4**

**Key Point:** The above formulae is applicable to all transistor configuration. Only we have added the appropriate subscript to h-parameters corresponding to the transistor configuration in the expression of \( A_i \), \( A_v \), \( Z_i \) and \( Y_o \).

Table 2.5 shows the typical values of h parameters for three different configurations at normal room temperature and at quiescent operating point \( I_{EQ} = 7.3 \text{ mA} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CE</th>
<th>CC</th>
<th>CB</th>
</tr>
</thead>
<tbody>
<tr>
<td>( h_{11} = h_i )</td>
<td>1100 Ω</td>
<td>1100 Ω</td>
<td>21.6 Ω</td>
</tr>
<tr>
<td>( h_{12} = h_r )</td>
<td>25 \times 10^{-4}</td>
<td>-1</td>
<td>29 \times 10^{-4}</td>
</tr>
<tr>
<td>( h_{21} = h_f )</td>
<td>50</td>
<td>-51</td>
<td>-0.98</td>
</tr>
<tr>
<td>( h_{22} = h_o )</td>
<td>25 μA / V</td>
<td>25 μA / V</td>
<td>0.49 μA / V</td>
</tr>
</tbody>
</table>

**Table 2.5**

2.10.3 Method for Analysis of a Transistor Circuit

In the previous section we have seen generalized transistor circuit analysis using h-parameters. There are many transistor circuits. Circuits may consist of different biasing techniques, different configurations and so on. The analysis of such transistor circuits for its small signal behaviour can be made by following simple guidelines. These guidelines are:
1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace d.c. source by a short circuit. In other words, short $V_{CC}$ and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its $h$-parameter model.

Following example explains us how to use guidelines for the analysis of a transistor circuit.

Consider a common emitter amplifier with voltage divider bias circuit as shown in the Fig. 2.52 (a)

**Guideline 1**: Draw actual circuit diagram

![Actual circuit diagram](image1)

![Circuit with capacitors as a short circuit](image2)

*Fig. 2.52 (a) & (b)*

**Guideline 2**: Short coupling and bypass capacitors.

**Guideline 3**: Short $V_{CC}$ and ground lines.

**Guideline 4**: Mark points B, C, E and locate these points as the start of the equivalent circuit.

![Circuit with $V_{CC}$ and ground short circuit](image3)

![Circuit with B, C and E points located](image4)

*Fig. 2.52*

**Guideline 5**: Replace transistor by its $h$-parameter model

and calculate effective $R_i (R'_i)$ and effective $R_o (R'_o)$.

For example, in above circuit $R'_i = R_1 \parallel R_2 \parallel R_i$

and $R'_o = R_o \parallel R_C$. 
With these guidelines we will analyze CE, CB and CC amplifier circuits in coming sections.

Fig. 2.52 (e) Circuit with transistor replaced by h-parameter equivalent

Example 2.11: Consider a single stage CE amplifier with \( R_s = 1 \ \text{k}\Omega, R_1 = 50 \ \text{K}, \ R_2 = 2 \ \text{K}, R_C = 1 \ \text{K}, R_L = 1.2 \ \text{K}, h_{fe} = 50, h_{ie} = 1.1 \ \text{K}, h_{oe} = 25 \ \mu\text{A/V and} \ h_{re} = 2.5 \times 10^{-4} \), as shown in Fig. 2.53.

Find \( A_v, R_p, A_o, A_i = \frac{I_L}{I_S}, A_{VS} = \frac{V_o}{V_S} \) and \( R_o \).

Solution:

Fig. 2.54
a) Current gain

\[ A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1 + h_{oe}R_L} \]

where \( R'_L = R_C \parallel R_L = 1 \text{ K} \parallel 1.2 \text{ K} = 545.45 \Omega \)

\[ \therefore A_i = \frac{-50}{1 + 25 \mu A / V(545.45)} = -49.32 \]

b) Input resistance

\[ R_i = h_{re} + h_{re} A_i R'_L \]

\[ = 1.1 \text{ K} + 2.5 \times 10^{-4} \times (-49.32) \times 545.45 \]

\[ = 1093 \Omega \]

c) Voltage gain

\[ A_v = \frac{V_c}{V_b} = \frac{A_i R'_L}{R_i} = \frac{-49.32 \times 545.45}{1093} = -24.61 \]

d) Overall input resistance

\[ R'_i = R_i \parallel R_1 \parallel R_2 = 1093 \parallel 50 \text{ K} \parallel 2 \text{ K} = 696.9 \Omega \]

e) Overall voltage gain

\[ A_{vs} = \frac{V_c}{V_s} = \frac{V_c}{V_b} \times \frac{V_b}{V_s} \]

Looking at Fig. 2.55 and voltage divider equation we get,

\[ V_b = \frac{V_i}{R_s + R'_i} \therefore \frac{V_b}{V_s} = \frac{R'_i}{R_s + R'_i} \]

\[ \therefore A_{vs} = \frac{V_c}{V_b} \times \frac{V_b}{V_s} = A_v \times \frac{R'_i}{R_s + R'_i} = 24.61 \times \frac{696.9}{1 \text{ K} + 696.9} = 10.1 \]

f) \[ A_i (\text{for circuit}) = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} \]

Looking at Fig. 2.56 and 2.57 and using current divider equation we have,

\[ I_L = \frac{-I_c R_C}{R_C + R_L} \]

\[ \therefore \frac{I_L}{I_c} = \frac{-R_C}{R_C + R_L} \]

and \[ I_b = \frac{I_s R_B}{R_B + R_i} \]
where \( R_B = R_1 \parallel R_2 = 50 \text{ K} \parallel 2 \text{ K} = 1.923 \text{ K} \)

\[
\therefore \quad \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i}
\]

\[
\therefore \quad A_i (\text{for circuit}) = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} = \frac{-R_C}{R_C + R_L} \times 49.32 \times \frac{R_B}{R_B + R_i}
\]

\[
= \frac{-1 \text{ K}}{1 \text{ K} + 1.2 \text{ K}} \times 49.32 \times \frac{1.923 \text{ K}}{1.923 \text{ K} + 1.093 \text{ K}} = -14.29
\]

\[
Y_o = h_{oc} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}
\]

where \( R_s' = R_s \parallel R_1 \parallel R_2 = 1 \text{ K} \parallel 50 \text{ K} \parallel 2 \text{ K} \)

\[
= 25 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{1.1 \times 10^3 + 657.9} = 1.7889 \times 10^{-5}
\]

\[
R_o = Z_o = \frac{1}{Y_o} = 55.899 \text{ k}\Omega
\]

\[
R_o' = R_o \parallel R_L
\]

\[
= 55.899 \text{ k}\Omega \parallel 545.45
\]

\[
= 540 \text{ \Omega}
\]

**Example 2.12:** In the common collector in Fig. 2.58, the transistor parameters are \( h_{ic} = 1.2 \text{ K}, h_{fe} = -101, h_{re} = 1 \) and \( h_{oc} = 25 \mu A / V \). Calculate the \( R_o \), \( A_i = \frac{I_L}{I_s} \), \( A_{ov} = \frac{V_o}{V_s} \), \( R_o \) for the circuit.

**Solution:** Fig. 2.59 shows the \( h \)-parameters equivalent model for the given circuit.
Fig. 2.59 h-parameter equivalent model

a) Current gain
\[ A_i = \frac{I_e}{I_b} = \frac{-h_{fe}}{1 + h_{oc}R'_L} \text{ where } R'_L = R_E \parallel R_L \]
\[ = \frac{-(-101)}{1 + 25 \times 10^{-6} (5 \text{ K} \parallel 20 \text{ K})} = 91.81 \]

b) Input resistance
\[ (R_i) = h_{ic} + h_{re} A_i R'_L \]
\[ = 1.2 \text{ K} + 1 \times 91.81 \times (5 \text{ K} \parallel 20 \text{ K}) = 368.44 \text{ K} \]

c) Overall input resistance
\[ R'_i = R_i \parallel R_1 \parallel R_2 = 368.44 \text{ K} \parallel 10 \text{ K} \parallel 10 \text{ K} = 4.933 \text{ K} \]

d) Voltage gain
\[ (A_v) = \frac{A_i R'_L}{R_1} = \frac{91.81 \times (5 \text{ K} \parallel 20 \text{ K})}{368.44 \text{ K}} = 0.996 \]

e) Overall voltage gain (A_{vs})
\[ \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s} \]
\[ \text{ where } \frac{V_o}{V_b} = A_v \text{ and } \frac{V_o}{V_s} = \frac{R'_i}{R'_i + R_s} \]
\[ \therefore \quad A_{vs} = A_v \cdot \frac{R'_i}{R'_i + R_s} = 0.996 \times \frac{4.933 \text{ K}}{4.933 \text{ K} + 1 \text{ K}} = 0.828 \]

f) Overall current gain
\[ (A_{ib}) = \frac{I_L}{I_s} = \frac{I_L}{I_e} \times \frac{I_e}{I_b} \times \frac{I_b}{I_s} \]
\[ \text{ where } \frac{I_L}{I_e} = \frac{-R_E}{R_E + R_L} = \frac{-5 \text{ K}}{5 \text{ K} + 20 \text{ K}} = -0.2 \]
\[ \frac{I_e}{I_b} = -A_i = -91.81 \]
\[ \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(101110)}{(101110) + 368.44} = 0.0134 \]
\[ \therefore \quad A_{ib} = \frac{I_L}{I_s} = (-0.2) \times (-91.81) \times (0.0134) = 0.246 \]

g) Output resistance
\[ R_o = \frac{1}{h_{oc}h_{re}} \text{ where } R'_2 = R_s \parallel R_1 \parallel R_2 = 833.33 \Omega \]
\[ \therefore \quad R_o = \frac{1}{25 \times 10^{-6} \left( \frac{-101 \times 1}{1.2 \text{ K} + 833.33} \right)} = 20.12 \Omega \]
\[ R'_o = R_o \parallel R'_L = 20.12 \parallel (5 \text{ K} \parallel 20 \text{ K}) = 20 \Omega \]
Example 2.13: For the common base circuit in Fig. 2.62, the transistor parameters are $h_{ib} = 22 \, \Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49 \, \mu A/V$, $h_{ib} = 2.9 \times 10^{-4}$. Calculate the values of the input resistance, output resistance, current gain and voltage gain for the given circuit.

![Fig. 2.62](image)

Solution: Fig. 2.63 shows the h-parameter equivalent model for the given circuit.

![Fig. 2.63](image)

a) Current gain

\[
(A_i) = -\frac{h_{fb}}{1 + h_{ob} R'_L} \quad \text{where} \quad R'_L = R_C \parallel R_L
\]

\[
= \frac{10 \, \Omega \parallel 12 \, \Omega}{1 + 0.49 \times 10^{-6} \times 5.45 \, \Omega} = -0.977
\]

b) Input resistance

\[
(R'_i) = h_{ib} + h_{be} A_i R'_L
\]

\[
= 22 \, \Omega + 2.9 \times 10^{-4} \times (-0.977) \times (5.45 \, \Omega) = 20.45 \, \Omega
\]

\[
R'_i = R_i \parallel R_E = 20.45 \parallel 5\Omega = 20.36 \, \Omega
\]

c) Voltage gain

\[
(A_v) = \frac{A_i R'_i}{R_i} = \frac{(-0.977) \times (5.45 \, \Omega)}{20.45} = -260
\]

d) Overall voltage gain

\[
A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_e} \times \frac{V_e}{V_s} \quad \text{where} \quad \frac{V_o}{V_e} = A_v \quad \frac{V_e}{V_s} = \frac{R'_i}{R'_i + R_s}
\]

\[
A_{vs} = A_v \frac{R'_i}{R'_i + R_s} = -260 \times \frac{20.36}{20.36 + 1 \, \text{K}} = -5.18
\]

e) Overall current gain

\[
A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_e} \times \frac{I_e}{I_s} = \frac{I_L}{I_C}
\]

\[
= -\frac{R_C}{R_C + R_L} = -\frac{10 \, \text{K}}{10 \, \text{K} + 12 \, \text{K}} = -0.454
\]
\[ \frac{I_C}{I_e} = -A_i = 0.977 \]
\[ \frac{I_C}{I_s} = \frac{R_E}{R_E + R_I} = \frac{5 \text{ K}}{5 \text{ K} + 20.45} = 0.996 \]

\( A_i \) (for circuit) = \((-0.454) \times (0.977) \times 0.996 = 0.442 \)

f) Output resistance \( (R_o) = \frac{1}{h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R'_s}} \)

where \( R'_s = R_s \parallel R_E = 1 \text{ K} \parallel 5 \text{ K} = 833.33 \Omega \)

\[
= \frac{1}{0.49 \times 10^{-6} - \left(\frac{-0.98 \times 2.9 \times 10^{-4}}{22 + 833.33}\right)} = 1.21 \text{ M}\Omega
\]

\( R'_o = R_o \parallel R'_f = 1.21 \text{ M} \parallel 5.45 \text{ K} = 5.425 \text{ K} \)

From Table 2.4 we can write the generalized formulae for common emitter, common collector and common base configurations. However, in most of the times h-parameters are specified for common emitter configuration, therefore, for analysis of common collector and common base configurations we have to first convert given h-parameters for common emitter configuration into the desired configuration by using conversion formulae given in Table 2.6.

**h-parameter conversion table:**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Common emitter</th>
<th>Common collector</th>
<th>Common base</th>
<th>T equivalent circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( h_{ie} )</td>
<td>1,100 ( \Omega )</td>
<td>( h_{ic} * )</td>
<td>( \frac{h_{ib}}{1 + h_{fb}} )</td>
<td>( r_b + \frac{r_c}{1 - a} )</td>
</tr>
<tr>
<td>( h_{re} )</td>
<td>25 ( \times 10^{-4} )</td>
<td>1 - ( h_{re} * )</td>
<td>( \frac{h_{ib} h_{ob}}{1 + h_{fb} - h_{rb}} )</td>
<td>( \frac{r_b}{(1 - a) r_c} )</td>
</tr>
<tr>
<td>( h_{fe} )</td>
<td>50</td>
<td>- (1 + ( h_{fe} )) *</td>
<td>( - h_{fb} )</td>
<td>( \frac{a}{1 - a} )</td>
</tr>
<tr>
<td>( h_{oe} )</td>
<td>25 ( \mu A / V )</td>
<td>( h_{oe} * )</td>
<td>( \frac{h_{ob}}{1 + h_{fb}} )</td>
<td>( \frac{1}{(1 - a) r_c} )</td>
</tr>
<tr>
<td>( h_{ib} )</td>
<td>( \frac{h_{ie}}{1 + h_{fe}} )</td>
<td>( \frac{h_{ie}}{h_{fe}} )</td>
<td>21.8 ( \Omega )</td>
<td>( r_c + (1 - a) r_b )</td>
</tr>
<tr>
<td>( h_{rb} )</td>
<td>( \frac{h_{ie} h_{oe}}{1 + h_{fe} - h_{re}} )</td>
<td>( h_{be} * )</td>
<td>( \frac{h_{ic} h_{oc}}{h_{fe} - 1} )</td>
<td>( r_b )</td>
</tr>
<tr>
<td>( h_{gb} )</td>
<td>( \frac{h_{fe}}{1 + h_{fe}} )</td>
<td>( - \frac{1 + h_{fe}}{h_{fe}} )</td>
<td>- 0.98</td>
<td>- a</td>
</tr>
<tr>
<td>( h_{eb} )</td>
<td>( \frac{h_{oe}}{1 + h_{fe}} )</td>
<td>( \frac{h_{oe}}{h_{fe}} )</td>
<td>0.49 ( \mu A / V )</td>
<td>( \frac{1}{r_c} )</td>
</tr>
<tr>
<td>( h_{ic} )</td>
<td>( h_{ie} * )</td>
<td>1,100 ( \Omega )</td>
<td>( \frac{h_{ib}}{1 + h_{fb}} )</td>
<td>( r_b + \frac{r_c}{1 - a} )</td>
</tr>
<tr>
<td>( h_{re} )</td>
<td>( 1 - h_{re} = 1 ) *</td>
<td>1</td>
<td>1</td>
<td>( 1 - \frac{\tau_c}{(1-a)\tau_c} )</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>( h_{fe} )</td>
<td>( -(1 + h_{fe}) ) *</td>
<td>-51</td>
<td>( \frac{1}{1 + h_{fb}} )</td>
<td>( \frac{1}{1 - a} )</td>
</tr>
<tr>
<td>( h_{oc} )</td>
<td>( h_{oc} ) *</td>
<td>25 ( \mu A / V )</td>
<td>( \frac{h_{ob}}{1 + h_{fb}} )</td>
<td>( \frac{1}{(1 - a)\tau_c} )</td>
</tr>
<tr>
<td>( a )</td>
<td>( \frac{h_{fe}}{1 + h_{fe}} )</td>
<td>( \frac{1 + h_{fe}}{h_{fe}} )</td>
<td>-( h_{fb} )</td>
<td>0.980</td>
</tr>
<tr>
<td>( \tau_c )</td>
<td>( \frac{1 + h_{fe}}{h_{oc}} ) *</td>
<td>-( \frac{h_{fe}}{h_{oc}} ) *</td>
<td>( \frac{1}{h_{ob}} )</td>
<td>2.04 M</td>
</tr>
<tr>
<td>( \tau_c )</td>
<td>( \frac{h_{oc}}{h_{oc}} ) *</td>
<td>( \frac{1 - h_{re} \tau_c}{h_{oc} \tau_c} )</td>
<td>( h_{ob} + \frac{h_{fb}}{h_{ob}} (1 + h_{fb}) ) *</td>
<td>10 ( \Omega )</td>
</tr>
<tr>
<td>( f_b )</td>
<td>( h_{oc} + \frac{h_{re}}{h_{oc}} (1 + h_{fe}) ) *</td>
<td>( h_{ic} + \frac{h_{fe}}{h_{oc}} (1 + h_{re}) ) *</td>
<td>( \frac{h_{ob}}{h_{ob}} ) *</td>
<td>590 ( \Omega )</td>
</tr>
</tbody>
</table>

* Exact

### 2.10.4 Analysis using Simplified Hybrid Model

So far we have seen the exact calculations of current gain, voltage gain, input and output impedances of transistor amplifier circuits. In most practical cases it is appropriate to obtain approximate values of current gain, voltage gain, input and output impedances rather than to carry out more lengthy exact calculations. We can justify this statement with the fact that h-parameter themselves usually vary widely for the same type of transistor. But now the question is when to use approximate analysis? To solve this question there is a generalized rule. This rule says that if \( h_{oc} \cdot R_L < 0.1 \) then we can proceed for approximate analysis; otherwise do the exact analysis. In this section we see how to analyze transistor with approximate model.

#### 2.10.4.1 Analysis of Common Emitter Circuit using Simplified Hybrid Model

Let us consider the h-parameter equivalent circuit for the amplifier, as shown in the Fig. 2.66.

Now, see how can we modify this model so as to make the analysis simple without greatly sacrificing accuracy?

Since \( 1/h_{oc} \) is in parallel with \( R_L \) and \( R_C \) if \( 1/h_{oc} >> R_L || R_C \), then \( h_{oc} \) may be neglected. If we neglect \( h_{oc} \), the collector current \( I_c \) is given by

\[
I_c = h_{fe} I_b
\]

Under these conditions the magnitude of the voltage of the generator in the emitter circuit is,

\[
h_{re} |V_{ce}| = h_{re} I_c (R_L || R_C) = h_{re} h_{fe} I_b (R_L || R_C)
\]

Since \( h_{re} h_{fe} = 0.01 \), this voltage may be neglected in comparison with the \( h_{fe} I_b \) drop across \( h_{ie} \), provided that \( R_L || R_C \) is not too large. We therefore conclude that if the load resistance \( R_L || R_C \) is small, it is possible to neglect the parameters \( h_{re} \) and \( h_{oc} \) in the h-parameter equivalent circuit. Fig. 2.67 shows the approximate h-parameter equivalent circuit.
Current gain: From Table 2.4 the CE current gain is given as

$$A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1+h_{oe}R_L}$$

By neglecting $h_{oe}$ we have,

$$A_i = -h_{fe} \quad \ldots(1)$$

Input impedance: From Table 2.4 the CE input impedance is given as

$$R_i = h_{ie} + h_{re} A_i R_L$$

By neglecting $h_{re}$ we have,

$$R_i = h_{ie} \quad \ldots(2)$$

Voltage gain: From Table 2.4 the voltage gain is given as

$$A_v = \frac{A_i R_L}{R_i} = \frac{A_i R_L}{h_{ie}} \quad \ldots(3)$$

Output impedance: From Table 2.4 the CE output impedance is given as

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}$$

By neglecting $h_{oe}$ and $h_{re}$

$$Y_o = 0$$

$$R_o = \frac{1}{Y_o} = \infty \quad \ldots(4)$$

$$R_o' = R_o || R_L = \infty || R_L = R_L \quad \ldots(5)$$

**Example 2.14**: Consider a single stage CE amplifier with $R_s = 1 \, K$, $R_1 = 50 \, K$, $R_2 = 2 \, K$, $R_C = 2 \, K$, $R_L = 2 \, K$, $h_{fe} = 50$, $h_{ie} = 1.1 \, K$, $h_{oe} = 25 \, \mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$, as shown in Fig. 2.68.

Find $A_i$, $R_i$, $A_v$, $A_o = \frac{I_L}{I_o}$, $A_{vs} = \frac{V_o}{V_s}$ and $R_o'$. 

![Fig. 2.68](image-url)
Solution: Since \( h_{\text{re}} R'_i = 25 \times 10^{-6} \times (2 \, \Omega \parallel 2 \, \Omega) = 0.025 \), which is less than 0.1, we use approximate analysis.

Fig. 2.69 shows the simplified hybrid model for the given circuit.

![Fig. 2.69](image)

**Simplified hybrid model**

a) Current gain \( (A_i) = -h_{\text{re}} = -50 \)

b) Input impedance \( (R'_i) = h_{\text{re}} = 1.1 \, \Omega \)

\[
R'_i = h_{\text{re}} \parallel R_1 \parallel R_2 = 1.1 \, \Omega \parallel 2.1 \, \Omega = 2 \, \Omega
\]

\[
R'_i = 700 \, \Omega
\]

c) Voltage gain \( (A_v) = \frac{A_i R'_L}{R_i} = \frac{-50 \times (2 \, \Omega \parallel 2 \, \Omega)}{1.1 \, \Omega} = -45.45 \)

d) Output impedance \( (R_o) = \frac{1}{V_o} = \infty \)

\[
R'_o = R_0 \parallel R'_i = \infty \parallel 2 \, \Omega = 2 \, \Omega
\]

e) Overall voltage gain \( (A_{V_o}) = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s} \)

where \( \frac{V_o}{V_b} = A_v \) and \( \frac{V_b}{V_s} = \frac{R'_i}{R'_i + R_s} \)

\[
A_{V_o} = \frac{A_v R'_i}{R'_i + R_s} = \frac{-45.45 \times 700}{700 + 1 \, \Omega} = -18.71
\]

f) Overall current gain \( A_i = \frac{I_o}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} \)

\[
\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = -\frac{1 \, \Omega}{1 \, \Omega + 1 \, \Omega} = -0.5
\]

\[
\frac{I_c}{I_b} = h_{\text{re}} = 50
\]

Looking at Fig. 2.71

\[
\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(50 \, \parallel 2)}{(50 \, \parallel 2) + 1.1} = 0.636
\]

\[
A_i \text{ (for circuit)} = \frac{I_L}{I_s} = -0.5 \times 50 \times 0.636 = -15.9
\]
2.10.4.2 Analysis of Common Collector Circuit using Simplified Hybrid Model

We have seen the simplified CE model, in which input is applied to base and output is taken from collector, and emitter is common between input and output. The same simplified model can be modified to get simplified CC model. For simplified CC model, we have to make collector common and take the output from emitter, as shown in the Fig. 2.72. The $h_{fe} I_b$ current direction is now exactly opposite that of CE model because the current $h_{fe} I_b$ always points towards emitter.

![Fig. 2.72 Simplified CC model](image-url)

Current gain: It is defined as the ratio of output to input currents

$$A_i = \frac{I_o}{I_b} = -\frac{-I_e}{I_b} = 1 + h_{fe} \quad \ldots(6)$$

Input resistance:

From Fig. 2.72 we obtain

$$R_i = \frac{V_b}{I_b}$$

Applying KVL we have

$$V_b - I_b h_{fe} - I_o R_L = 0$$

$$\therefore \quad V_b = I_b h_{fe} + I_o R_L$$

$$\therefore \quad \frac{V_b}{I_b} = h_{fe} + \frac{I_o}{I_b} R_L$$

$$\therefore \quad R_i = \frac{V_b}{I_b} = h_{fe} + (1 + h_{fe}) R_L$$

$$\therefore \quad \frac{I_o}{I_b} = -\frac{-I_e}{I_b} = 1 + h_{fe} \quad \ldots(7)$$

The above equation shows that input impedance of CC is higher than the CE configuration.

Voltage gain ($A_v$):

It is given as

$$A_v = \frac{V_o}{V_b} = \frac{I_o R_L}{I_b R_i} = \frac{A_i R_L}{R_i} \quad \therefore \quad A_i = \frac{I_o}{I_b} = -\frac{I_e}{I_b} \quad \ldots(8)$$
Substituting values of $A_v$ and $R_i$ we get

$$A_v = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L} \approx 1 \text{ but always less than } 1 \quad \therefore (1 + h_{fe}) R_L \gg h_{ie} \quad \ldots (9)$$

**Output resistance $R_o$**:

It is the ratio of output voltage $V_o$ to output current $I_e$ with $V_s = 0$

$$R_o = \frac{V_o}{I_e} \bigg|_{V_s=0}$$

Applying KVL we have,

$$V_s - I_b R_s - I_b h_{ie} - V_o = 0$$

$$\therefore \quad V_o = -I_b R_s - I_b h_{ie} \quad \therefore V_s = 0 = -I_b (R_s + h_{ie})$$

$$I_e = -(1 + h_{fe}) I_b$$

$$\therefore \quad V_o = \frac{-I_b (R_s + h_{ie})}{I_e} = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

$$\therefore \quad R_o = \frac{V_o}{I_e} = \frac{R_s + h_{ie}}{1 + h_{fe}} \quad \ldots (10)$$

The output resistance $R_o$ of the stage, taking the load into account is given as

$$R_o = R_o || R_L \quad \ldots (11)$$

**Example 2.15**: A common collector circuit as shown in Fig. 2.73 has the following components: $R_1 = 27 \text{k}\Omega, R_2 = 27 \text{k}\Omega, R_E = 5.6 \text{k}\Omega, R_L = 47 \text{k}\Omega, R_s = 600 \text{ \Omega}$. The transistor parameters are $h_{ie} = 1 \text{k}\Omega, h_{fe} = 85$ and $h_{oe} = 2 \mu\text{A/V}$. Calculate $A_i, R_T, A_{pv}, R_{pv}, A_{vs} = \frac{V_o}{V_s}$ and $A_t = \frac{I_o}{I_s}$.

![Fig. 2.73](image)
Solution: Here, \( h_{oc} \times R'_L = 2 \times 10^{-6} \times (5.6 \parallel 47 \, \text{K}) = 0.01 \), which is less than 0.1. Thus we analyse the circuit with approximate method.

Fig. 2.74 shows the simplified hybrid model for the given circuit.

**Fig. 2.74 Simplified hybrid model**

a) Current gain
\[
(A_i) = 1 + h_{fe} = 1 + 85 = 86
\]

b) Input resistance
\[
(R_i) = h_{ie} + (1 + h_{fe}) \frac{R'_L}{R'_L = h_{ie} + (1 + h_{fe}) (R_E \parallel R_L)}
\]
\[
= 1\, \text{K} + (1 + 85) (5.6 \parallel 47 \, \text{K}) = 431.33 \, \text{k}\Omega
\]
\[
R'_i = R_1 \parallel R_1 \parallel R_2 = 431.33 \, \text{K} \parallel 27 \, \text{K} \parallel 27 \, \text{K} = 13.09 \, \text{K}
\]

c) Voltage gain
\[
(A_v) = \frac{(1+h_{fe}) R'_i}{h_{ie} + (1+h_{fe}) R'_L}
\]
\[
= \frac{(1+85) (5.6 \parallel 47 \, \text{K})}{1 \, \text{K} + (1+85) (5.6 \parallel 47 \, \text{K})} = 0.997
\]

d) Output resistance

Looking Fig. 2.74 the output resistance
\[
R_o = \frac{R'_o + h_{ie}}{1+h_{fe}} = \frac{(R_1 \parallel R_2 \parallel R_3) + h_{ie}}{1+h_{fe}}
\]
\[
= \frac{(27 \, \text{K} \parallel 27 \, \text{K} \parallel 600) + 1 \, \text{K}}{1+85} = 18.3 \, \Omega
\]
\[
R'_o = R_o \parallel R_E \parallel R_L = 18.3 \parallel 5.6 \, \text{K} \parallel 47 \, \text{K} = 18.23 \, \Omega
\]

e) Overall voltage gain
\[
A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s} = \frac{V_o}{V_s} \times \frac{V_b}{V_s}
\]

where \( \frac{V_o}{V_b} = A_v \) and \( \frac{V_b}{V_s} = \frac{R'_i}{R'_i + R_s} \)

\[
A_{vs} = \frac{A_v R'_i}{R'_i + R_s} = \frac{0.997 \times 13.09 \, \text{K}}{13.09 \, \text{K} + 600} = 0.953
\]
f) Overall current gain

\[ A_i = \frac{I_o}{I_s} = \frac{I_o}{I_e} \times \frac{I_e}{I_b} \times \frac{I_b}{I_s} \]

where \( \frac{I_o}{I_e} = \frac{-R_E}{R_E + R_L} = \frac{-5.6 \text{ K}}{5.6 \text{ K} + 47 \text{ K}} = -0.106 \)

\[ \frac{I_e}{I_b} = (1 + h_{fe}) = -86 \]

Looking at Fig. 2.75

\[ \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(27 \text{ K} \ || \ 27 \text{ K})}{(27 \text{ K} \ || \ 27 \text{ K}) + 431.33 \text{ K}} = 0.03 \]

\[ \therefore A_i \text{ (for circuit)} = \frac{I_o}{I_s} = (-0.106) \times (-86) \times (0.03) = 0.273 \]

2.10.4.3 Analysis of Common Base Circuit using Simplified Model

The approximate CB model can be drawn by giving input to emitter, taking output from collector and making base common. The Fig. 2.76 shows the approximate CB model.

Current gain (\( A_i \)) : It is defined as a ratio of output to input currents

\[ \therefore A_i = \frac{I_o}{I_e} = \frac{-I_c}{I_e} = \frac{-h_{fe} I_b}{-(1 + h_{fe}) I_b} \quad \therefore I_c = h_{fe} I_b \text{ and } I_e = -(1 + h_{fe}) I_b \]

\[ \therefore A_i = \frac{h_{fe}}{1 + h_{fe}} \quad \text{...(12)} \]

The above equation of CB shows that its current gain is always less than one.

Input resistance (\( R_i \)) :

It is defined as ratio of input voltage to input current

\[ R_i = \frac{V_e}{I_e} = \frac{-h_{ie} I_b}{-(1 + h_{fe}) I_b} \quad \therefore V_e = -h_{ie} I_b \text{ and } I_e = -(1 + h_{fe}) I_b \]

\[ = \frac{h_{ie}}{1 + h_{fe}} \quad \text{...(13)} \]

The above equation of CB shows that its input resistance is very low as compare to CE and CC configurations.
**Voltage gain** \((A_v)\) : It is defined as a ratio of output to input voltages

\[
A_v = \frac{V_o}{V_e} = I_o \frac{R_L}{I_c R_i} = \frac{A_i R_L}{R_1}
\]

Substituting value of \(A_i\) and \(R_1\) we get,

\[
A_v = \frac{h_fe \times R_L}{1 + h_fe} = \frac{h_fe R_L}{h_{ie}}
\] ...\((14)\)

**Output resistance** \((R_o)\) : It is the ratio of output voltage to output current at

\[
V_s = 0
\]

\[
R_o = \left. \frac{V_o}{I_c} \right|_{V_s=0}
\]

When \(V_s = 0\), the current through input loop \(I_b = 0\), hence \(I_c = 0\) and \(R_o = \infty\).

The output resistance \(R_o^'\) of the stage, taking the load into account is given as

\[
R_o^' = R_o \parallel R_L = \infty \parallel R_L = R_L
\] ...\((15)\)

**Example 2.16** : A common base amplifier, as shown in Fig. 2.77 has the following components : \(R_e = 600 \Omega\), \(R_C = 5.6 \, \text{k}\Omega\), \(R_E = 5.6 \, \text{k}\Omega\), \(R_L = 39 \, \text{k}\Omega\). The transistor parameters are \(h_{ie} = 1 \, \text{k}\), \(h_{fe} = 85\) and \(h_{oe} = 2 \, \mu\text{A/V}\). Calculate \(R_v\), \(R_o\), \(A_v\), \(A_{26}\) = \(\frac{V_o}{V_s}\)

![Fig. 2.77](image)

**Solution** : Since \(h_{oe} \times (R_C \parallel R_L) = 2 \times 10^{-6} \times (5.6 \, \text{k}\Omega \parallel 39 \, \text{k}\Omega) = 9.79 \times 10^{-3}\), which is less than 0.1, we use approximate analysis method. The Fig. 2.78 shows the simplified hybrid model for the given circuit.

![Fig. 2.78 Simplified hybrid model](image)
Current gain \( (A_I) = \frac{h_{fe}}{1 + h_{fe}} = \frac{85}{1+85} = 0.988 \)

Input resistance \( (R_I) = \frac{h_{ie}}{1 + h_{ie}} = \frac{1000}{1+85} = 11.627 \Omega \)

\[ R_I' = R_I \parallel R_E = 11.627 \parallel 5.6 \, \text{K} = 11.6 \, \Omega \]

Voltage gain \( (A_v) = \frac{h_{fe}R_L}{h_{ie}} = \frac{85 \times (5.6 \, \text{K} \parallel 39 \, \text{K})}{1 \, \text{K}} = 416.23 \]

Output resistance \( (R_o) = \infty \)

\[ R_o' = R_o \parallel R_L = R_o \parallel R_C \parallel R_L = \infty \parallel 5.6 \, \text{K} \parallel 39 \, \text{K} = 4.89 \, \text{K} \]

\[ A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_e} \times \frac{V_e}{V_s} = A_v \times \frac{V_e}{V_s} \]

where

\[ \frac{V_e}{V_s} = \frac{R_I'}{R_I' + R_s} \]

\[ \therefore \quad A_{vs} = A_v \times \frac{R_I'}{R_I' + R_s} = 416.23 \times \frac{11.6}{11.6 + 600} = 7.89 \]

2.9 Analysis of Common Emitter Amplifier with Collector to Base Bias

The Fig. 2.47 shows the common emitter amplifier with collector to base bias. As shown in the Fig. 2.47, the resistance \( R_F \) in this configuration is connected between input and output. For the analysis of this circuit it is necessary to split this resistance for input and output. This can be achieved by using Miller’s theorem.

![Fig. 2.47](image-url)
2.9.1 Miller's Theorem

In general, the Miller theorem is used for converting any circuit having configuration of Fig. 2.48 (a) to another configuration shown in Fig. 2.48 (b).

The Fig. 2.48 shows that, if Z is the impedance connected between two nodes, node 1 and node 2, it can be replaced by two separate impedances \( Z_1 \) and \( Z_2 \); where \( Z_1 \) is connected between node 1 and ground and \( Z_2 \) is connected between node 2 and ground.

The \( V_i \) and \( V_o \) are the voltages at the node 1 and node 2 respectively. The values of \( Z_1 \) and \( Z_2 \) can be derived from the ratio of \( V_o \) and \( V_i \) \((V_o / V_i)\), denoted as \( K \). Thus it is not necessary to know the values of \( V_i \) and \( V_o \) to calculate the values of \( Z_1 \) and \( Z_2 \).

The values of impedances \( Z_1 \) and \( Z_2 \) are given as

\[
Z_1 = \frac{Z}{1-K} \quad \ldots (1)
\]

and

\[
Z_2 = \frac{Z \cdot K}{K-1} \quad \ldots (2)
\]

2.9.2 Proof of Miller's Theorem

Miller's theorem states that, the effect of resistance \( Z \) on the input circuit is a ratio of input voltage \( V_i \) to the current \( I \) which flows from the input to the output.

Therefore,

\[
Z_1 = \frac{V_i}{I}
\]

where,

\[
I = \frac{V_i - V_o}{Z} = \frac{V_i \left[ 1 - \frac{V_o}{V_i} \right]}{Z} = \frac{V_i [1 - A_v]}{Z}
\]

\[
\therefore \quad Z_1 = \frac{V_i}{I} = \frac{Z}{1-A_v} = \frac{Z}{1-K} \quad \therefore \quad \frac{V_o}{V_i} = A_v = K
\]

Miller's theorem states that, the effect of resistance \( Z \) on the output circuit is a ratio of output voltage \( V_o \) to the current \( I \) which flows from the output to the input.
Therefore,
\[ Z_2 = \frac{V_o}{I} \]
where,
\[ I = \frac{V_o - V_i}{Z} = \frac{V_o \left[ 1 - \frac{V_i}{V_o} \right]}{Z} = \frac{V_o \left[ 1 - \frac{1}{A_v} \right]}{Z} \]
\[ = \frac{V_o \left[ \frac{A_v - 1}{A_v} \right]}{Z} \]
\[ \therefore Z_2 = \frac{V_o}{I} = \frac{Z}{A_v - 1} = \frac{ZA_v}{A_v - 1} = \frac{ZK}{K-1} \]
\[ \therefore \frac{V_o}{V_i} = A_v = K \]

**Miller Effect Capacitance**

In inverting amplifiers, the capacitive element, \( C_f \), is connected between input and output terminals of the active device i.e., \( X_{C_f} = \frac{1}{j\omega C_f} \). The large capacitors will control the low-frequency response due to their low reactance levels.

Therefore, the Miller effect input capacitance \( C_{Mi} \), is derived as
\[ Z_i = \frac{Z}{(1 - A)} \]
i.e.
\[ \frac{1}{j\omega C_{Mi}} = \frac{1}{j\omega C_f (1 - A)} \]

Therefore,
\[ C_{Mi} = (1 - A)C_f \]

Hence, it is evident that, in any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance, \( C_f \), between the input and output terminals of the active device.

The Miller output capacitance, \( C_{Mo} \), is derived as
\[ Z_o = \frac{Z}{(1 - \frac{1}{A})} \]
i.e.
\[ \frac{1}{j\omega C_{Mo}} = \frac{1}{j\omega C_f \left( 1 - \frac{1}{A} \right)} \]

Therefore,
\[ C_{Mo} = \left( 1 - \frac{1}{A} \right) C_f \]
If \( A \gg 1 \), \( C_{Mo} = C_f \)
**Dual of Miller’s theorem** Dual of Miller’s theorem states that if an impedance \( Z \) connected as shunt element between input and output terminals, as shown in Fig. 1.38(a) can be replaced by an impedance \( Z_0 = Z(1 - A_f) \) at the input side and \( Z_0 = Z \left( 1 - \frac{1}{A_f} \right) = Z \left( \frac{A_f - 1}{A_f} \right) \) at the output side as shown in Fig. 1.38(b), where the current ratio, \( A_j = \frac{I_2}{I_1} \). This can be verified by finding that the voltage across \( Z_i \) is \( I_1 Z_i \) which is equal to the voltage drop \((I_1 + I_2)Z\) across \( Z \) if \( Z_i = Z(1 - A_f) \). Hence the input voltage \( V_i \) is the same in the two circuits in Fig. 1.38(a) and (b).

Similarly the voltage \( V_2 \) has the same value in the two circuits if the impedance \( Z_o = \left[ \frac{A_f - 1}{A_f} \right] Z \). Therefore, the two networks are identical. This transformation is useful in the analysis of electric circuits.

![Fig. 1.38 Dual of Miller’s theorem](image)

**2.9.3 Analysis using Miller’s Theorem**

For the common emitter amplifier with collector to base bias shown in Fig. 2.51, calculate \( R_1, A_i, A_v, A_v \) and \( R_o \). The transistor parameters are \( h_{ie} = 1.1 \, K, h_{fe} = 50, h_{ce} = h_{re} = 0. \)

**h-parameter equivalent circuit**: The Fig. 2.51 shows the approximate h-parameter equivalent circuit for the amplifier shown in Fig. 2.52.

![Fig. 2.51](image)
Applying Miller's theorem we get simplified circuit as shown in the Fig. 2.52. The voltage $A_v$ of the circuit can be given as $\frac{V_o}{V_i}$. As the amplifier is a common emitter amplifier we can assume that the voltage gain $A_v >> 1$, i.e. $K >> 1$. This assumption makes it easier to calculate the value of $Z_2$. $Z_2$ is given as,

$$Z_2 = \frac{Z \cdot K}{K-1} = \frac{Z \cdot K}{K} \quad \therefore K >> 1$$

$$= Z$$

$$\therefore Z_2 = Z = 200 \text{ k}\Omega$$

![Fig. 2.52 Simplified h-parameter equivalent circuit using Miller's theorem](image)

However, we do not know the exact value of $A_v$, thus we cannot calculate exact value of $Z_1$ at this stage.

**Analysis:**

Since $h_{oe} = h_{re} = 0$, we use approximate analysis

a) **Current gain** ($A_i$)

$$A_i = -h_{fe} = -50$$

b) **Input resistance** ($R_i$)

$$R_i = h_{ie} = 1.1 \text{ k}\Omega$$

c) **Voltage gain** ($A_v$)

$$A_v = \frac{A_i R'_L}{R_i} \quad \text{where} \quad R'_L = Z_2 || R_L = 200 \text{ K} || 10 \text{ K} = 9.52 \times 10^3$$

$$\therefore A_v = \frac{-50 \times 9.52 \times 10^3}{1.1 \times 10^3} = -432.72$$

d) **Overall input resistance** ($R'_i$)

$$R'_i = Z_1 || R_i \quad \text{where} \quad Z_1 = \frac{Z}{1 - K} = \frac{Z}{1 - A_v} = \frac{200 \text{ K}}{1 - (-432.72)} = 461.12 \text{ K}$$

$$= 461.12 || 1100 = 324.9 \text{ K}$$
e) Overall voltage gain \((A_{VS})\)

\[
A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}
\]

Looking at Fig. 2.52 we have,

\[
\frac{V_i}{V_s} = \frac{R'_i}{R'_i + R_s} = \frac{324.9}{324.9 + 1000} = 0.245
\]

\[\therefore A_{VS} = A_v \times 0.245 = -432.72 \times 0.245 = -106\]

f) Overall current gain \((A_I)\)

\[
A_I = \frac{I_o}{I_i} = \frac{I_o}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_i}
\]

Looking at Fig. 2.54 we have,

\[
\frac{I_o}{I_c} = \frac{-Z_2}{Z_2 + R_L} = -\frac{200}{200 + 10} = -0.952
\]

and \[
\frac{I_b}{I_i} = \frac{Z_1}{Z_1 + R'_i} = \frac{461.12}{461.12 + 1100} = 0.295
\]

\[\therefore A_I = \frac{I_o}{I_i} = -0.952 \times 50 \times 0.295 = -14\]

g) Output resistance

\[
R_o = \infty
\]

\[
R'_o = \infty || R_L = \infty || 9.52 K = 9.52 K
\]

2.10 Analysis of Common-Emitter Amplifier with an Emitter Resistance

Whenever the gain provided by a single stage amplifier is not sufficient, it is necessary to cascade the number of stages of the amplifier. In such situations, it becomes important to stabilize the voltage amplification of each stage, because instability of the first stage is amplified in the second stage and it is further amplified in the next. This is not desired. The simple and effective way to obtain voltage gain stabilization is to add an emitter resistance \(R_E\) to a CE stage as shown in Fig. 2.55. The presence of emitter resistance has number of better effects on the amplifier performance. These effects can be analysed with the help of h-parameter equivalent circuit.
Fig. 2.56 A.C. equivalent circuit for common emitter circuit with unbypassed emitter

### 2.10.1 Approximate Analysis

An approximate analysis of the common emitter circuit with $R_E$ can be made using approximate $h$-parameter equivalent circuit shown in Fig. 2.57.

**Fig. 2.57 Approximate model for CE amplifier with $R_E$**

**Current Gain ($A_i$) :** The current gain can be given as

$$A_i = \frac{-I_C}{I_B} = \frac{-h_{fe}I_B}{I_B} = -h_{fe} \quad \ldots(5)$$

**Input Resistance ($R_i$) :** Look at Fig. 2.57 we can write input resistance as

$$R_i = \frac{V_i}{I_B} = h_{ie} + (1 + h_{fe}) R_E \quad \ldots(6)$$

The input resistance due to factor $(1 + h_{fe}) R_E$ may be very much larger than $h_{ie}$. Hence an emitter resistance greatly increases the input resistance.

**Voltage Gain ($A_v$) :** It is given as

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E} \quad \ldots(7)$$

**Output Resistance ($R_o$) :** It is the resistance of an amplifier without considering the source and load (i.e. $V_s = 0$ and $R_L = \infty$). It is defined as a ratio of output voltage $V_o$ to output current with $V_s = 0$. 

---

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\[ R_o = \frac{V_o}{I_o} \bigg|_{V_s=0} \]

When \( V_s = 0 \), the current through the input loop \( I_b = 0 \), hence \( I_c \) and \( I_o \) both are zero. Therefore, \( R_o = \infty \). The output resistance \( R'_o \) of the stage, taking the load into account is given as

\[ R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L \] ... (8)

**Example 2.7**: Fig. 2.58 shows a single stage CE amplifier with unbypassed emitter resistance find current gain, input resistance, voltage gain and output resistance. Use typical values of h-parameter

![Fig. 2.58](image)

**Solution**: Typical values for h-parameters are \( h_{fe} = 50 \), \( h_{ie} = 1.1 \ K \), \( h_{oe} = 25 \ \mu A/V \), \( h_{re} = 2.5 \times 10^{-4} \). Since \( h_{oe} R_L = 25 \times 10^{-6} \times (1 \ K \parallel 1.2 \ K) = 0.0136 \), which is less than 0.1, we use approximate analysis.

![Fig. 2.58 (a) Approximate h-parameter equivalent circuit](image)

**a) Current Gain**

\[ (A_i) = \frac{-I_c}{I_b} = -h_{fe} = -50 \]

**b) Input Resistance**

\[ (R_i) = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe}) R_E \]

\[ = 1.1 \ K + (1 + 50) \times 270 = 14.87 \ K \]
c) Overall Voltage Gain

\[ A_v = \frac{A_i R_L}{R_i} = \frac{-50 \times (1.2 \, \text{K} \| 1 \, \text{K})}{14.87 \, \text{K}} = -1.834 \]

d) Overall Input Resistance

\[ (R'_i) = R_i \| R_1 \| R_2 = 14.87 \, \text{K} \| 50 \, \text{K} \| 2 \, \text{K} = 1.7 \, \text{K} \]

e) Output Resistance

\[ (R'_o) = R_o \| R_c \| R_L = \infty \| 1 \, \text{K} \| 1.2 \, \text{K} = 545.45 \, \Omega \]

f) Overall Voltage Gain

\[ A_{vs} = \frac{A_v R'_i}{R'_i + R_s} = \frac{-1.834 \times 1.7 \, \text{K}}{1.7 \, \text{K} + 1 \, \text{K}} = -1.15 \]

g) Overall current gain

\[ A_i = \frac{I_L}{I_c} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} \]

where

\[ \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(50 \| 2)}{(50 \| 2) + 14.87} = 0.1145 \]

Looking at Fig. 2.58 (b) we can write

\[ \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(50 \| 2)}{(50 \| 2) + 14.87} = 0.1145 \]

\[ A_i \text{(for circuit)} = \frac{I_L}{I_s} = -0.454 \times 50 \times 0.1145 = -2.6 \]

2.11 Comparison of Transistor Configurations

<table>
<thead>
<tr>
<th>Sr.No.</th>
<th>Characteristic</th>
<th>Common Base</th>
<th>Common Emitter</th>
<th>Common Collector</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Input resistance</td>
<td>Very low (20 Ω)</td>
<td>Low (1 kΩ)</td>
<td>High (500 kΩ)</td>
</tr>
<tr>
<td>2.</td>
<td>Output resistance</td>
<td>Very high (1 MΩ)</td>
<td>High (40 kΩ)</td>
<td>Low (50 Ω)</td>
</tr>
<tr>
<td>3.</td>
<td>Input current</td>
<td>( I_E )</td>
<td>( I_B )</td>
<td>( I_B )</td>
</tr>
<tr>
<td>4.</td>
<td>Output current</td>
<td>( I_C )</td>
<td>( I_C )</td>
<td>( I_E )</td>
</tr>
<tr>
<td>5.</td>
<td>Input voltage applied</td>
<td>Emitter and Base</td>
<td>Base and Emitter</td>
<td>Base and Collector</td>
</tr>
<tr>
<td>6.</td>
<td>Output voltage taken</td>
<td>Collector and Base</td>
<td>Collector and Emitter</td>
<td>Emitter and Collector</td>
</tr>
<tr>
<td>7.</td>
<td>Current amplification factor</td>
<td>( \alpha = \frac{I_C}{I_E} )</td>
<td>( \beta = \frac{I_C}{I_B} )</td>
<td>( \gamma = \frac{I_E}{I_B} )</td>
</tr>
<tr>
<td>8.</td>
<td>Current gain</td>
<td>Less than unity</td>
<td>High (20 to few hundreds)</td>
<td>High (20 to few hundreds)</td>
</tr>
<tr>
<td>9.</td>
<td>Voltage gain</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>10.</td>
<td>Applications</td>
<td>As a input stage of multistage amplifier</td>
<td>For audio signal amplification</td>
<td>For impedance matching</td>
</tr>
</tbody>
</table>
Emitter Follower:

Common Collector Configuration of BJT amplifier is called Emitter Follower. The input is applied to the base, and the output is taken from the emitter. The common terminal for both the circuits is the collector.

- The above configuration is called as emitter follower because its voltage gain is nearly equal to unity i.e. $V_o \approx V_i$ which means change in input voltage is nearly equal to change in output voltage.
- In this configuration emitter follows the input signal. Here input resistance is very high i.e. in the range of kilos and output voltage is very low i.e. in the range of tens of ohms.
- Hence common use of common collector is as a buffer stage which transfers resistance from high to low resistance over a wide range of frequency with voltage gain of unity.
- It also increases the power level of signal.

\[
A_I = -\frac{I_o}{I_b} = -\frac{h_{fe}}{1 + h_{oc} R_L}
\]

\[
Z_I = \frac{V_I}{I_b} = h_{ie} + h_{re} A_I R_L
\]

\[
A_V = \frac{V_o}{V_i} = A_I \frac{R_L}{R_I}
\]

\[
Y_o = h_{oc} - \frac{h_{fe} h_{re}}{h_{ie} + R_S} \quad \text{Where } R_S \text{ and } R_L \text{ is source and load resistance.}
\]
1.16 DESIGN OF SINGLE STAGE RC COUPLED AMPLIFIER USING BJT

A single-stage RC coupled CE amplifier shown in Fig. 1.39 can be employed as a small-signal amplifier but a circuit with two cascaded stage gives large amplification. The design of resistor values involves application of Ohm’s law after selecting suitable voltage and current levels throughout the circuit. The design of capacitor values are based on the lower cut-off frequency of the circuit and the resistance which is in series with the capacitor.

In this circuit, the biasing is provided by three resistors $R_1$, $R_2$ and $R_E$. The resistors $R_1$ and $R_2$ act as a potential divider giving a fixed voltage to the base. If collector current increases due to change in temperature or change in $h_{fe}$, then the emitter current $I_E$ also increases, reducing the voltage difference between base and emitter ($V_{RE}$). Due to reduction in $V_{RE}$, base current $I_B$ and hence collector current $I_C$ also reduces. Negative feedback acts in emitter bias circuit. This reduction in collector current $I_C$ compensated for the original change in $I_C$. The frequency response of the single-stage RC coupled BJT amplifier is shown in Fig. 1.40.

**Design of $R_C$ and $R_E$**

The design of single-stage RC coupled amplifier is based on the specifications like supply voltage, minimum voltage gain, frequency response, source impedance and load impedance. The circuit shown in Fig. 1.39 has no provision for negative feedback because of the bypass capacitor $C_E$ and hence it is designed to achieve the largest possible gain. The voltage gain of a CE amplifier circuit is given by

$$A_v = \frac{-h_{fe} (R_C \parallel R_L)}{h_{ie}}$$

Since $A_v$ is directly proportional to $R_C \parallel R_L$, the design for large voltage gain requires selection of the largest possible collector resistance. But a large value of $R_C$ needs the collector current to be small for satisfactory operation of transistor. The value of collector resistance $R_C$ can be determined by applying Kirchhoff’s voltage law around the collector-emitter circuit.

![Diagram](image)

**Fig. 1.40** Typical frequency response for a transistor amplifier
i.e.,

\[ V_{CC} = I_C R_C + V_{CE} + V_E \]

\[ R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}, \quad \text{where } V_E = I_E R_E \]

To achieve larger value of \( R_C \), let us assume \( V_{CE} = \frac{V_{CC}}{2} \) and \( V_E = \frac{V_{CC}}{10} \).

For good bias stability, the emitter resistor voltage drop, \( V_E \), should be greater than the base emitter voltage \( V_{BE} \) i.e., \( V_E > V_{BE} \). Since \( V_E = V_B - V_{BE} \), the emitter voltage \( V_E \) will be slightly affected by the variation in \( V_{BE} \) due to change in temperature.

Hence, \( I_E \) and \( I_C \) remain stable at \( I_C \approx I_E = \frac{V_E}{R_E} \).

**Analysis of a Voltage-Divider Bias Circuit**

By Ohm’s law, the input resistance at the transistor base is

\[ R_{\text{in(base)}} = \frac{V_{\text{in}}}{I_{\text{in}}} \]

Here

\[ V_{\text{in}} = V_{BE} + I_E R_E \]

\[ = I_E R_E, \quad \text{since } V_{BE} \ll I_E R_E \]

\[ \approx \beta I_B R_E, \quad \text{since } I_E \approx I_C = \beta I_B \]

and

\[ I_{\text{in}} = I_B. \]

Therefore,

\[ R_{\text{in(base)}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{\beta I_B R_E}{I_B} = \beta R_E \]

The total resistance from base to ground is

\[ R_2 \parallel R_{\text{in(base)}} = R_2 \parallel \beta R_E \]

A voltage divider is formed by \( R_1 \) and the resistance from base to ground, \( \beta R_E \), in parallel with \( R_2 \). Therefore,

\[ V_B = \left( \frac{R_2 \parallel \beta R_E}{R_1 + R_2 \parallel \beta R_E} \right) V_{CC} \]

If \( \beta R_E \gg R_2 \) (at least 10 times greater), then

\[ V_B = \left( \frac{R_2}{R_1 + R_2} \right) V_{CC}. \]
Design of Bias Resistors

The voltage divider current \( I_2 \) is selected as \( \frac{I_C}{10} \) which results in good bias stability and high input resistance. Hence, the bias resistors are calculated as

\[
R_2 = \frac{V_B}{I_2} \quad \text{and} \quad R_1 = \frac{V_{CC} - V_B}{I_2} \quad \text{where} \quad V_B = V_E + V_{BE} \quad \text{or} \quad V_B = \left( \frac{R_2}{R_1 + R_2} \right) V_{CC}.
\]

Design of Bypass and Coupling Capacitors

Always the bypass capacitor across the emitter resistor is used to filter out the signal variations at the emitter with respect to ground. Therefore the reactance offered by this capacitor should be low for high frequencies but high for dc and nearby low frequencies.

\[
X_{C_E} = \frac{1}{2\pi f C_E}
\]

where \( X_{C_E} \) should be high for dc and very low frequency signals and low for high frequencies. Therefore,

\[
C_E = \frac{1}{2\pi f X_{C_E}}
\]

where \( C_E \) should be high for high frequencies starting from 100 Hz.

Therefore, \( X_{C_E} \) can be fixed at one-tenth of \( R_E \).

All capacitors should be selected to have the smallest possible capacitance value mainly to minimize the physical size of the circuit. Each capacitor has its highest impedance at the lowest operating frequency and it is calculated based on the lower cut-off frequency. The bypass capacitor \( C_E \) is normally the largest capacitor in the circuit. We known that the voltage gain for CE circuit with unbypassed emitter resistance given by

\[
A_v = \frac{-h_{fe}(R_C \parallel R_L)}{h_{fe} + R_E(1 + h_{fe})}
\]

By including the bypass capacitor in parallel with \( R_E \) the voltage gain is given by

\[
A_v = \frac{-h_{fe}(R_C \parallel R_L)}{h_{fe} + R_E(1 + h_{fe})(R_E \parallel X_{C_E})}
\]

Normally \( R_E \gg X_{C_E} \) so \( R_E \) can be neglected and also \( X_{C_E} \) is capacitive reactance.

Hence,

\[
A_v = \frac{-h_{fe}(R_C \parallel R_L)}{\sqrt{h_{fe}^2 + [(1 + h_{fe}) (X_{C_E})]^2}}
\]

When \( h_{fe} = (1 + h_{fe})X_{C_E} \)

\[
|A_v| = \frac{-h_{fe}(R_C \parallel R_L)}{h_{fe} \sqrt{1^2 + 1^2}} = \frac{A_{vm}}{\sqrt{2}},
\]

where \( A_{vm} \) is the mid frequency gain.
Therefore, at lower cut-off frequency \( f_L \),

\[ h_{ic} = (1 + h_{fe}) X_{C_e}. \]

Hence,

\[ X_{C_e} = \frac{h_{ic}}{1 + h_{fe}}. \]

We know that

\[ \frac{h_{ic}}{1 + h_{fe}} = h_{ib}. \]

Therefore,

\[ C_E = \frac{1}{2\pi f_L X_{C_e}} = \frac{1}{2\pi f_L h_{ib}}. \]

The coupling capacitors \( C_1 \) and \( C_2 \) have negligible effect on the frequency response of the amplifier circuit and to minimize the effects of these capacitors, the reactance of each coupling capacitor is selected to be approximately equal to one-tenth of the impedance in series with it at the lower cut-off frequency \( f_L \). These capacitances can be determined from the equations given by

\[ C_1 = \frac{1}{2\pi f_L X_{C_1}}, \quad \text{where} \quad X_{C_1} = \frac{Z_i}{10} = \frac{(R_1 \parallel R_2 \parallel h_{fe})}{10}, \]

and

\[ C_2 = \frac{1}{2\pi f_L X_{C_2}}, \quad \text{where} \quad X_{C_1} = \frac{Z_O}{10} = \frac{R_C \parallel R_L}{10}. \]

Example 1.12 Design a single stage RC coupled BJT amplifier circuit shown in Fig. 1.39. Assume that \( V_{CC} = 10 \text{ V}, I_C = 4 \text{ mA, } h_{fe} = 100, h_{ie} = 1 \text{ k}\Omega, R_L = 100 \text{ k}\Omega \) and \( f_L = 100 \text{ Hz}. \)

Solution

Refer to Fig. 1.39.

(a) To determine bias resistors \( R_1 \) and \( R_2 \) and \( R_C \) and \( R_E \)

We know that

\[ V_E = \frac{V_{CC}}{10} = \frac{10}{10} = 1 \text{ V}, \quad V_{CE} = \frac{V_{CC}}{2} = 5 \text{ V}. \]

\[ \frac{V_{CC}}{10} = V_C = V_{CE} + V_E \]

Therefore, \( I_C R_C = V_{CC} - V_{CE} - V_E = 10 - 5 - 1 = 4 \text{ V} \)

i.e

\[ R_C = \frac{4}{4 \times 10^{-3}} = 1 \text{ k}\Omega \]

Here, \( V_E = I_E R_E = I_C R_E \)

Therefore,

\[ R_E = \frac{V_E}{I_C} = \frac{1}{4 \times 10^{-3}} = 250 \Omega \]

\[ V_B = V_{BE} + V_E = 0.7 + 1 = 1.7 \]

\[ V_B = \left( \frac{R_2}{R_1 + R_2} \right) V_{CC} \]
\[ \frac{R_2}{R_1 + R_2} = \frac{V_B}{V_{CC}} = \frac{1.7}{10} = 0.17 \]

\[ R_2 = 0.17(R_1 + R_2) \]

\[ 5.88R_2 = R_1 + R_2 \]

\[ 4.88R_2 = R_1 \]

The value of \( R_2 \) can be selected to satisfy \( \beta R_E \gg R_2 \). Hence \( R_2 \) is selected as \( 2 \, \text{k}\Omega \). Therefore, \( R_1 = 9.76 \, \text{k}\Omega = 10 \, \text{k}\Omega \)

(b) To determine the bypass capacitor \( C_E \)

\[ X_{C_E} = \frac{h_{ie}}{1 + h_{fe}} = \frac{1 \times 10^3}{1 + 100} = 9.9 \]

\[ C_E = \frac{1}{2\pi f_L X_{C_E}} = \frac{1}{2\pi \times 100 \times 9.9} = \frac{1}{6217.2} = 0.1608 \, \mu\text{F} \]

(c) To determine coupling capacitors \( C_1 \) and \( C_2 \)

\[ X_{C_1} = \frac{Z_i}{10} = \frac{(R_i \parallel R_2 \parallel h_{ie})}{10} = \frac{(10 \times 10^3 \parallel 2 \times 10^3 \parallel 1 \times 10^3)}{10} = 246.154 \]

\[ C_1 = \frac{1}{2\pi f_L X_{C_1}} = \frac{1}{2\pi \times 100 \times 246.154} = 6.47 \, \mu\text{F} \]

\[ X_{C_2} = \frac{Z_O}{10} = \frac{R_C \parallel R_L}{10} = \frac{1 \times 10^3 \parallel 100 \times 10^3}{10} = 99.001 \]

\[ C_2 = \frac{1}{2\pi f_L X_{C_2}} = \frac{1}{2\pi \times 100 \times 99.001} = \frac{1}{62172.628} = 0.1608 \, \mu\text{F} \]

JFET Amplifiers:

JFET amplifiers provide an excellent voltage gain with the added advantages of a high input impedance. Because of their high input impedance and other characteristics JFETs are often preferred over BJTs for certain types of applications.

Many of the concepts that relate to amplifiers using BJTs apply equally to FET amplifiers. There are three basic FET circuit configurations:

- Common source
- Common drain and
- Common gate.

These are similar to the bipolar transistor common emitter, common collector and common base circuits, respectively. The only difference is that BJT controls a large output (collector) current by means of a relative small input (base current), whereas, FET controls an output (drain) current by means of small input (gate) voltage. It is important to note that in both the cases the output current is the controlled variable.
4.3 JFET Low Frequency Small Signal Model

The JFET parameters are the major components of low frequency small signal model for JFET. Hence before examining the low frequency small signal model we recall the JFET parameters which we have studied earlier in chapter 1.

We know that, drain to source current of JFET is controlled by gate to source voltage. The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor $g_m$. It is given as

$$\Delta I_d = g_m \Delta V_{GS}$$  \hspace{1cm} (1)

We know that, in BJT the relation between an output and input quantity is given by amplification factor $\beta$, whereas in JFET this relation is given by transconductance factor $g_m$.

The another important parameter of JFET is drain resistance $r_d$. It is given by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \bigg|_{V_{GS} = \text{constant}}$$  \hspace{1cm} (2)

It determines the output impedance $Z_o$ of the JFET amplifier.

**JFET Low Frequency a.c. Equivalent Circuit**

Fig. 4.3 shows the small signal low frequency a.c. equivalent circuit for n-channel JFET. The relation of $I_d$ by $V_{gs}$ is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current $I_g$ is zero. The output impedance is represented by $r_d$ from drain to source.

![Fig. 4.3 JFET low frequency ac equivalent circuit for n-channel JFET](image)

**Fig. 4.3 JFET low frequency ac equivalent circuit for n-channel JFET**

**Key Point:** The lower case subscripts represent a.c. levels.

**Approximate a.c. Equivalent Circuit**

When the value of external drain resistance $R_D$ is very small as compared to the value of output impedance represented by $r_d$, it is possible to replace $r_d$ by open circuit. This gives us approximate a.c. equivalent circuit of JFET amplifier, as shown in Fig. 4.4.

![Fig. 4.4 Approximate a.c. equivalent circuit for JFET amplifier](image)
3.4 Common Source Circuit

In common source amplifier circuit input is applied between gate and source and output is taken from drain and source. In the following sections we see the low frequency equivalent circuits for common source configuration with different biasing techniques.

3.4.1 JFET with Fixed Bias

Fig. 3.5 shows common source amplifier with fixed bias. The coupling capacitor $C_1$ and $C_2$ which are used to isolate the d.c. biasing from the applied a.c. signal act as short circuits for the a.c. analysis.

![Common source JFET amplifier with fixed bias](image)

**Fig. 3.5** Common source JFET amplifier with fixed bias

Fig. 3.6 shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing:

- All capacitors and d.c. supply voltages with short circuits and
- JFET with its low frequency equivalent circuit.

![A.C. equivalent model for the common source amplifier circuit with fixed bias](image)

**Fig. 3.6** A.C. equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

**Input impedance $Z_i$**:

Looking into Fig. 3.5 we can say that,

$$Z_i = R_G$$

... (1)
**Output Impedance** $Z_o$:

The output impedance $Z_o$ is the impedance measured looking from the output side with input voltage ($V_i$) equal to 0. As $V_i = 0$,

$$V_{gs} = 0 \text{ and hence } g_m V_{gs} = 0.$$  

![Diagram](image)

Fig. 3.7

The $g_m V_{gs} = 0$ allows current source to be replaced by an open circuit, as shown in the Fig. 3.6 Therefore the output impedance is

$$Z_o = R_D || r_d \quad \ldots (2)$$

If the resistance $r_d$ is sufficiently large compared to $R_D$, then we say that the output impedance is approximately equal to $R_D$.

$$Z_o \approx R_D \quad \therefore r_d >> R_D \quad \ldots (3)$$

**Voltage Gain** $A_v$:

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. 3.5 we can write

$$V_o = -g_m V_{gs} \ (r_d || R_D) \quad \ldots (4)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \ (r_d || R_D) \quad \ldots (5)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m \ (r_d || R_D) \quad \ldots (6)$$

and if $r_d >> R_D$,

$$A_v = -g_m R_D \quad \ldots (7)$$

**Key Point:** The negative sign in the equation for $A_v$ clearly indicates there is a phase shift of 180° between input and output voltages.

Table 3.1 summarizes performance of common source amplifier with fixed bias.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Exact</th>
<th>With $r_d &gt;&gt; R_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_i$</td>
<td>$R_G$</td>
<td>$R_G$</td>
</tr>
<tr>
<td>$Z_o$</td>
<td>$R_D</td>
<td></td>
</tr>
<tr>
<td>$A_v$</td>
<td>$-g_m \ (R_D</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.1
Example 3.1: For the circuit shown in Fig. 3.8. Determine i) Input impedance ii) Output impedance and iii) Voltage gain.

Solution:

i) We have,

\[ Z_i = R_G = 1 \, \text{M} \Omega \]

ii) We have,

\[ Z_o = r_d || R_D = 50 \, \text{K} || 5.1 \, \text{K} = 4628 \, \Omega \]

iii) Voltage Gain \( A_v \) : We have,

\[ A_v = -g_m \cdot (r_d || R_D) = -2 \, \text{mS} \cdot (50 \, \text{K} || 5.1 \, \text{K}) = -2 \, \text{mS} \cdot (4628) = -9.256 \]

Example 3.2: For the circuit shown in the Fig. 3.9 \( V_{GSQ} = -2V \) with \( I_{DSS} = 8 \, mA \) and \( V_P = -8 \, V \). Calculate \( g_m, r_d, Z_i, Z_o \) and \( A_v \). The value of \( Y_{os} \) is given as \( 20 \, \mu \text{S} \).
Solution:

i) $g_m$ : We have,

$$g_m = \frac{g_{m0}}{V_T} = \frac{2 \times 10^{-3}}{8V} = 2 \text{ mS}$$

Also we have,

$$g_m = g_m \left( 1 - \frac{V_{GS}}{V_T} \right) = 2 \text{ mS} \left( 1 - \frac{-2V}{-8V} \right) = 1.5 \text{ mS}$$

ii) $r_d$ :

$$r_d = \frac{1}{\frac{1}{Y_{OE}}} = \frac{1}{20 \mu \Omega} = 50 \text{ k}\Omega$$

iii) $Z_i$ : We have,

$$Z_i = R_G = 1 \text{ M}\Omega$$

iv) $Z_o$ : We have,

$$Z_o = r_d || R_D = 50 \text{ K} || 5.1 \text{ K} = 4628 \Omega$$

v) $A_v$ : We have,

$$A_v = \frac{V_o}{V_i} = -g_m (r_d || R_D) = -1.5 \text{ mS} (50\text{K} || 5.1\text{K}) = -1.5 \text{ mS} (4628)$$

$$= -6.942$$

3.4.2 JFET with Self Bias (Bypassed $R_s$)

Fig. 3.10 shows common source amplifier with self bias.

The coupling capacitor $C_1$ and $C_2$ which are used to isolate the dc biasing from the applied a.c. signal act as short circuits for the low frequency analysis. Bypass capacitor $C_s$ also acts as a short circuit for the low frequency analysis.

![Common source JFET amplifier with self bias](image)

**Fig. 3.10 Common source JFET amplifier with self bias**

Fig. 3.11 shows the low frequency equivalent model for the common source amplifier circuit with self bias. It is drawn by replacing

- All capacitors and d.c. supply $V_{DD}$ with short circuits and,
- JFET with its low frequency equivalent circuit.
Fig. 3.11 a.c. equivalent model for the common source amplifier circuit with self bias

Since the resulting low frequency equivalent circuit is same as a.c. equivalent circuit in Fig. 3.6, the equation for $Z_i$, $Z_o$ and $A_v$ will also be same.

i) Input impedance $Z_i$ :
$$Z_i = R_G \quad \ldots \quad (8)$$

ii) Output impedance $Z_o$ :
$$Z_o = r_d || R_D \quad \ldots \quad (9)$$
if $r_d >> R_D$
$$Z_o \approx R_D \quad \ldots \quad (10)$$

iii) Voltage gain $A_v$ :
$$A_v = -g_m \left( r_d || R_D \right) \quad \ldots \quad (11)$$
If $r_d >> R_D$
$$A_v = -g_m R_D \quad \ldots \quad (12)$$

The negative sign in the equation (11) and (12) again indicates there is a phase shift of $180^\circ$ between input and output voltages.

3.4.3 JFET with Self Bias (Unbypassed $R_s$)

Fig. 3.12 shows common source amplifier with self biasing having unbypassed $R_s$.

![Diagram](image)

Fig. 3.12 Common source JFET amplifier with self bias having unbypassed $R_s$

Now $R_s$ will be the part of low frequency equivalent model as shown in the Fig. 3.13.

![Diagram](image)

Fig. 3.13 Low frequency equivalent model for the common source amplifier circuit with self bias having unbypassed $R_s$
**Input impedance** $Z_i$:

Looking into Fig. 3.13 we can say that,

$$Z_i = R_G$$

... (13)

**Output impedance** $Z_o$:

It is given by

$$Z_o = Z_o' || R_D$$

...(14)

where

$$Z_o' = \frac{V_o}{I_d} \bigg|_{V_i = 0}$$

... (15)

Applying KVL on output circuit we get,

$$V_o = (I_d - g_m V_{gs})I_d + I_d R_s$$

...(16)

Applying KVL on input circuit we get,

$$V_{gs} = V_{in} - I_d R_s$$

... (17)

Since $V_{in} = 0$ we have,

$$V_{gs} = -I_d R_s$$

... (18)

Substituting value of $V_{gs}$ in equation 3.16 we get,

$$V_o = \left(\left((I_d - g_m (-I_d R_s))I_d\right) + (I_d R_s)\right) = I_d \left(r_d + g_m R_s r_d + R_s\right)$$

$$\therefore Z_o' = \frac{V_o}{I_d} = r_d + g_m R_s r_d + R_s$$

... (19)

We have,

$$\mu = g_m r_d$$

$$\therefore Z_o' = r_d + \mu R_s + R_s$$

$$= r_d + R_s (\mu + 1)$$

... (20)

We observe that with unbypassed $R_s$ the output impedance of circuit is increased, compare to when it is bypassed.

We know that,

$$Z_o = Z_o' || R_D$$

$$\therefore Z_o = \left[ r_d + R_s (\mu + 1) \right] || R_D$$

... (21)

or

$$Z_o = \left[ r_d + R_s (g_m r_d + 1) \right] || R_D$$

... (22)

**Voltage Gain** $A_v$:

It is given by,

$$A_v = \frac{V_o}{V_i}$$

... (23)

We know that,

$$V_o = -I_d R_D$$

... (24)
Applying KVL to the output circuit as shown in Fig. 3.14 we have,

\[(I_d - g_m V_{gs}) r_d + I_d R_s + I_d R_D = 0\] ...................(25)

We know that, \[V_{gs} = V_{in} - I_d R_s\]

Substituting value of \(V_{gs}\) in equation (25) we get,

\[\left[ I_d - g_m (V_i - I_d R_s) \right] r_d + I_d R_s + I_d R_D = 0 \] ...........................(26)

\[\therefore I_d r_d - g_m V_i r_d + g_m I_d R_s r_d + I_d R_s + I_d R_D = 0 \] ...........................(27)

\[\therefore I_d (r_d + R_s + R_D + g_m R_s r_d) = g_m V_i r_d \] ...........................(28)

\[\therefore I_d = \frac{g_m V_i r_d}{r_d + R_s + R_D + g_m R_s r_d} \] ...........................(29)

From equation (24) we know that,

\[V_o = - I_d R_D \] ...........................(30)

Substituting value of \(I_d\) from equation (29) we get,

\[V_o = \frac{-g_m V_i r_d R_D}{r_d + R_s + R_D + g_m R_s r_d} \] ...........................(31)

\[\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_D}{r_d + R_s + R_D + g_m R_s r_d} \] ...........................(32)

Dividing numerator and denominator by \(r_d\) we get,

\[\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \] ...........................(33)

If \(r_d \gg R_s + R_D\)

\[A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s} \] ...........................(34)

**Key Point**: With unbypassed \(R_s\) voltage gain reduces.
Table 3.2 summarizes performance of common source amplifier with self bias.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Bypassed $R_S$</th>
<th>Unbypassed $R_S$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Exact</td>
<td>Exact</td>
</tr>
<tr>
<td>$Z_i$</td>
<td>$R_G$</td>
<td>$R_G$</td>
</tr>
<tr>
<td>$Z_o$</td>
<td>$R_D \parallel r_d$</td>
<td>$R_D$</td>
</tr>
<tr>
<td>$A_v$</td>
<td>$-g_m (R_D \parallel r_d)$</td>
<td>$-g_m R_D$</td>
</tr>
</tbody>
</table>

Table 3.2

Example 3.3: For common source amplifier as shown in Fig. 3.15 operating point is defined by $V_{GSQ} = -2.5$ V, $V_P = -6$ V and $I_{DSQ} = 2.5$ mA with $I_{DSS} = 8$ mA. Calculate $g_m$, $r_d$, $Z_i$, $Z_o$ and voltage gain $A_v$.

Solution:

i) $g_m$ : We have,

$$g_{mo} = \frac{2 I_{DSS}}{|V_P|} = \frac{2 \left(8 \times 10^{-3}\right)}{6} = 2.67 \text{ mS}$$

![Diagram]

Fig. 3.15

$$g_m = g_{mo} \left(1 - \frac{V_{GSQ}}{V_p}\right) = 2.67 \text{ mS} \left(1 - \frac{(-2.5\text{V})}{(-6\text{V})}\right) = 1.58 \text{ mS}$$
ii) \( r_d \):
\[
r_d = \frac{1}{Y_{os}} = \frac{1}{20 \text{ mS}} = 50 \text{ k}\Omega
\]

iii) \( Z_i \): From equation 13 we have,
\[
Z_i = R_G = 1 \text{ M}\Omega
\]

iv) \( Z_o \): We have,
\[
Z_o = \left[ r_d + R_s (g_m r_d + 1) \right] || R_D
\]
\[
= \left[ 50\text{K} + 1\text{K} (1.58 \text{mS} \times 50 \text{K} + 1) \right] || 2.2 \text{K} = 2163.4 \text{ \Omega}
\]

v) \( A_v \): We have,
\[
A_v = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} = \frac{-1.58 \text{mS} \times 2.2 \text{K}}{1 + 1.58 \text{mS} \times 1\text{K} + \frac{1\text{K} + 2.2 \text{K}}{50 \text{K}}}
\]
\[
= \frac{-3.476}{2.644} = -1.315
\]

3.4.4 **JFET with Voltage Divider Bias (Bypassed \( R_s \))**

Fig. 3.16 shows common source amplifier with voltage divider biasing.

![Fig. 3.16 Common source JFET amplifier with voltage divider bias](image)

The coupling capacitor \( C_1 \) and \( C_2 \) which are used to isolate the d.c. biasing from the applied a.c. signal act as short circuits for the low frequency analysis. Bypass capacitor \( C_s \) also acts as short circuit for the low frequency analysis.

Fig. 3.16 shows the low frequency equivalent model for the common source amplifier circuit with voltage divider bias. It is drawn by replacing:

- All capacitors and d.c. supply \( V_{DD} \) with short circuits and,
- JFET with its low frequency equivalent circuit
Fig. 3.17 Low frequency equivalent model for the common source amplifier circuit with voltage divider bias

Since the resulting low frequency equivalent circuit is the same as a.c. equivalent circuit in Fig. 3.6, the equation for $Z_i$, $Z_o$ and $A_v$ will be the same.

It is important to note that, here,

$$R_G = R_1 \parallel R_2 .$$

$$Z_i = R_G$$

$$= R_1 \parallel R_2$$

$$Z_o = r_d \parallel R_D$$

$$\text{if } r_d \gg R_D$$

$$Z_o = R_D$$

$$A_v = -g_m (r_d \parallel R_D)$$

$$\text{if } r_d \gg R_D$$

$$A_v = -g_m R_D$$

The negative sign in equation (39) again indicates there is a phase shift of 180° between input and output voltages.

3.4.5 JFET with Voltage Divider Bias (Unbypassed $R_s$)

Fig. 3.18 shows common source amplifier with voltage divider bias having unbypassed $R_s$. 

Fig. 3.18 Common source JFET amplifier with voltage divider bias having unbypassed $R_s$
Now $R_s$ will be the part of a.c. equivalent model as shown in the Fig. 3.19.

Fig. 3.19 Low frequency equivalent model for the common source amplifier circuit with voltage divider bias having unbypassed $R_s$

Since the resulting a.c. equivalent circuit is the same as a.c. equivalent circuit in Fig. 3.19, the equation for $Z_i$, $Z_o$ and $A_v$ will be the same.

It is important to note that, here, $R_G = R_1 \parallel R_2$.  

$$Z_i = R_G = R_1 \parallel R_2 \quad \ldots (40)$$

$$Z'_o = r_d + g_m R_s \quad \ldots (41)$$

or

$$Z'_o = r_d + R_s (\mu + 1) \quad \ldots (42)$$

$$Z_o = [r_d + g_m R_s r_d + R_s] \parallel R_D \quad \ldots (43)$$

or

$$Z_o = [r_d + R_s (\mu + 1)] \parallel R_D \quad \ldots (44)$$

$$A_v = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \quad \ldots (45)$$

or

$$A_v = \frac{-g_m R_D}{1 + g_m R_s} \quad \ldots (46)$$

Example 3.4 : For the amplifier shown in Fig. 3.20, calculate:

i) $A_v = \frac{V_o}{V_i}$

ii) $Z_i$

iii) $Z_o$

iv) $Z'_o$. Assume for FET $g_m = 2 \text{ mA/V}$, $r_d = 10 \text{ k}\Omega$

Fig. 3.20

Solution : The equivalent circuit for given circuit can be drawn as follows

Fig. 3.21

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i) \[ A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \]

where \( R_D = 50 \text{ K} \parallel 50 \text{ K} = 25 \text{ K} \)

\[ = \frac{-2 \times 25}{1 + 2 \times 1 + \frac{25}{10}} = -8.928 \]

ii) \( Z_i = R_G = 1 \text{ M} \Omega \)

iii) \( Z_o = [r_d + g_m R_s r_d + R_s] \parallel R_D = [10 \text{ K} + 2 \text{ ms} \times 1 \times 10^3 \times 10 \times 10^3 + 1 \times 10^3] \parallel 50 \text{ K} \)

\[ = 19.135 \text{ k} \Omega \]

iv) \( Z'_o = Z_o \parallel R_L = 19.135 \text{ K} \parallel 50 \text{ K} = 13.838 \text{ k} \Omega \)

Table 3.3 summarizes the performance of common source amplifier with voltage divider bias.

<table>
<thead>
<tr>
<th>( \text{Bypassed } R_s )</th>
<th>( \text{Exact} )</th>
<th>( r_d &gt;&gt; R_o )</th>
<th>( \text{Unbypassed } R_s )</th>
<th>( \text{Exact} )</th>
<th>( r_d &gt;&gt; R_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_i )</td>
<td>( R_i \parallel R_2 )</td>
<td>( R_i \parallel R_2 )</td>
<td>( Z_o )</td>
<td>( r_d \parallel R_D )</td>
<td>( R_D )</td>
</tr>
</tbody>
</table>

**Table 3.3**

**3.5 Common Drain Circuit (Source Follower)**

In common drain amplifier circuit input is applied between gate and source and output is taken between source and drain.

![Fig. 3.22 Common drain amplifier circuit](image)

Fig. 3.22 shows common drain configuration.

It shows that the output is taken from source and when the d.c. supply is replaced by its short circuit equivalent the drain is grounded and thus common between input and output.

In the common drain circuit the source voltage \( V_s \) is given as,

\[ V_s = V_G + V_{GS} \]
When a signal is applied to the JFET gate via \( C_G \), \( V_G \) varies with the signal. As \( V_{GS} \) is fairly constant and \( V_G = V_G + V_{GS} \), \( V_s \) varies with \( V_i \). For example, if \( V_i \) increases by 0.25 V, \( V_s \) also approximately increases by 0.25 V. Because the output voltage at the source \( (V_s) \) follows changes in the signal voltage applied to the gate, this circuit is also called as source follower.

Fig. 3.23 shows the low frequency equivalent model for the common drain amplifier circuit shown in Fig. 3.22.

This low frequency equivalent circuit can be simplified as shown in the Fig. 3.23.

![Diagram](image.png)

**Fig. 3.23 Low frequency equivalent model for common drain circuit**

**Input Impedance** \( Z_i \):

Looking at Fig. 3.24, \( Z_i \) can written as,

![Diagram](image.png)

**Fig. 3.24 Simplified low frequency equivalent model for common drain circuit**

\[
Z_i = R_G \quad \ldots (1)
\]

**Output Impedance** \( Z_o \):

It is given by,

\[
Z_o = Z'_o \parallel R_s \quad \ldots (2)
\]

where

\[
Z'_o = \frac{V_o}{I_d \mid V_i = 0} \quad \ldots (3)
\]

Applying KVL to the outer loop we can have,

\[
V_i + V_{gs} - V_o = 0 \quad \ldots (4)
\]

As

\[
V_i = 0, \quad V_{gs} = V_o \quad \ldots (5)
\]

Looking at Fig. 3.24 we can write that,

\[
g_m V_{gs} = I_d \quad \ldots (6)
\]
Substituting value of $V_{gs}$ from equation (5) in equation we get,

$$g_m V_o = I_d$$

(7)

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

(8)

$$\therefore Z_o = \frac{1}{g_m} || R_s$$

(9)

**Voltage Gain $A_v$:**

It is given by,

$$A_v = \frac{V_o}{V_i}$$

(10)

Looking at Fig. 3.24 we can write that,

$$V_o = - I_d \ (r_d \ || R_s )$$

(11)

and

$$I_d = g_m V_{gs}$$

(12)

$$\therefore V_o = - g_m V_{gs} \ (r_d \ || R_s )$$

(13)

Again from equation 4 we have,

$$V_i = - V_{gs} + V_o$$

$$= - V_{gs} + [ - g_m V_{gs} \ (r_d \ || R_s) ]$$

(14)

Substituting values of $V_o$ and $V_i$ from equations (13) and (14) respectively in above equation (10) we get,

$$A_v = \frac{- g_m V_{gs} \ (r_d \ || R_s )}{- V_{gs} \ (1 + g_m (r_d \ || R_s))}$$

$$= \frac{g_m (r_d \ || R_s)}{1 + g_m (r_d \ || R_s)}$$

(15)

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

(16)

if $g_m R_s >> 1$

$$A_v = 1$$, but it is always less than one.

(17)

**Key Point:**

1. *We observe that the common drain circuit does not provide voltage gain.*

2. *The positive sign in equation (16) also indicates that there is no phase shift between input and output voltages.*

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Table 3.4 summarizes the performance of common drain amplifier.

<table>
<thead>
<tr>
<th></th>
<th>Exact</th>
<th>( r_d \gg R_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_i )</td>
<td>( R_G )</td>
<td>( R_G )</td>
</tr>
<tr>
<td>( Z_o )</td>
<td>( \frac{1}{g_m} \parallel R_s )</td>
<td>( \frac{1}{g_m} \parallel R_s )</td>
</tr>
<tr>
<td>( A_v )</td>
<td>( \frac{g_m \left( r_d \parallel R_s \right)}{1 + g_m \left( r_d \parallel R_s \right)} )</td>
<td>( \frac{g_m R_s}{1 + g_m R_s} )</td>
</tr>
</tbody>
</table>

Table 3.4

Example 3.5: For common drain amplifier as shown in Fig. 3.25, \( g_m = 2.5 \text{ mS} \), \( r_d = 25 \text{ k}\Omega \). Calculate \( Z_i \), \( Z_o \) and \( A_v \).

Solution:

\( Z_i \): We have,

\[
Z_i = R_G = 1 \text{ M}\Omega
\]

\( Z_o \): We have,

\[
Z_o = \frac{1}{g_m} \parallel R_s = \frac{1}{2.5 \text{ mS}} \parallel 3.3 \text{ K} = \frac{400 \times 3.3 \text{ K}}{400 + 3.3 \text{ K}} = 356.76 \text{ \Omega}
\]

\( A_v \): We have,

\[
A_v = \frac{g_m \left( r_d \parallel R_s \right)}{1 + g_m \left( r_d \parallel R_s \right)} = \frac{2.5 \text{ mS} \left( 25 \text{ K} \parallel 3.3 \text{ K} \right)}{1 + 2.5 \text{ mS} \left( 25 \text{ K} \parallel 3.3 \text{ K} \right)}
\]

\[
= \frac{2.5 \text{ mS} \left( 2915.2 \right)}{1 + 2.5 \text{ mS} \left( 2915.2 \right)} = \frac{7.288}{1 + 7.288} = 0.879
\]