SIDDHARTH INSTITUTE OF ENGINEERING &TECHNOLOGY: PUTTUR

ELECTRONICS & COMMUNICATON ENGINEERING

VLSI DESIGN

QUESTION BANK

UNIT –I

Introduction

1.a) Explain the steps involved in fabrication of a p-well process CMOS transistor. [L2][CO1][7M]

b) List steps involved in n-well process. [L2][CO1][3M]

2. a) Explain clearly about Moore's law. [L2][CO1][3M]

b) With neat diagrams, explain the different steps in n-well fabrication of CMOS transistor. [L3][CO1][7M]

3.a) What is the need of VLSI circuits? [L2][CO1][2M]

b) Compare the relative merits of three different forms of pull up for an inverter circuit. What is the best choice for realization in (a) nMOS technology (b) CMOS technology? [L3] [CO1][8M]

4.a) Compare CMOS with Bipolar transistors in different aspects. [L2][CO1][3M]

b) Draw the circuit diagram of a simple BiCMOS inverter and explain its operation. [L2][CO1][7M]

5. Derive the relationship between I_{ds} & V_{ds} in non-saturated and saturated region. [L4][CO1][10M]

6.Explain the n-MOS fabrication steps with neat sketches and use p^+ masking. [L2][CO1][10M]

7.a) Explain the MOS Transistor operation of three conditions with the help of neat sketches [L2][CO1][5M]

b) Explain the operation of Bi-CMOS inverter and draw the different alternative structures. [L2][CO1][5M]

8.Write about the following

a) Transconductance ($g_{m)}$ and output conductance (g_{ds}). [L2][CO1][5M]

b) Figure of merit (ω_o). [L2][CO1][5M]

9.a) State why NMOS technology is preferred more than PMOS technology. [L1][CO1][5M]

b) Discuss the generations of Integration Circuits. [L1][CO1][5M]

10.Explain in details about different types of alternative pull-ups with neat sketches. [L2][CO1][10M]

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UNIT –II

VLSI Circuit Design Process

1. a) Explain the different steps involved VLSI Design flow. [L2][CO2][5M]
   b) What is a stick diagram? Draw the stick diagram of a three input CMOS NAND gate. [L3][CO2][5M]
2. a) What is lambda-based design rules. [L3][CO2][5M]
   b) Explain design rules for wires and MOS transistors. [L2][CO2][5M]
3. a) Explain 2µm -based design rules with neat sketches. [L2][CO2][5M]
   b) Draw a stick diagram and layout of NMOS inverter circuit. Both Input and Output points should be Polysilicon layer. [L3][CO2][5M]
4. a) Explain about Stick's diagram with suitable examples. [L2][CO2][5M]
   b) Draw the schematic and layout for 2-input NAND gate [L3][CO2][5M]
5. a) Draw the stick diagram for CMOS inverter? [L3][CO2][5M]
   b) Draw the layout diagram for CMOS inverter? [L3][CO2][5M]
6. a) Draw a stick diagram for $Y=(AB+CD)^{'}$ using NMOS design style. [L3][CO2][5M]
   b) Draw the schematic and layout diagram of 2-input NOR gate using CMOS deign style . [L3][CO2][5M]
7. Design a layout diagram for the CMOS logic
   a) y= [(a+b).c]'. [L3][CO2][5M]
   b) z= (ab+cd+e)' [L3][CO2][5M]
8. a) Draw the polysilicon and Metal type1 contact cut. [L2][CO2][5M]
   b) Explain how the p-MOS transistor forms in lambda-based design rules. [L2][CO2][5M]
9. a) Realize the layout of AND-OR-INVERTER in NMOS design Styles. [L4][CO2][5M]
   b) Write about Implant, demarcation line in stick diagrams with neat sketches. [L3][CO2][5M]
10. a)What is MOS layer? [L1][CO2][2M]
    b) Explain different types of MOS layers used in VLSI circuits. [L3][CO2][8M]

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UNIT –III

Gate Level Design &Physical Design

1. a) Draw the CMOS implementation of 2X1 mux using transmission gates. [L3][CO3][5M]
   b) Clearly explain the AOI implementation using CMOS design style with neat sketches. [L4][CO3][5M]
2. a) What is switch logic? [L2][CO3][3M]
   b) Explain about pass transistors and transmission gate. [L2][CO3][7M]
3. a) What is pseudo NMOS logic? [L2][CO3][5M]
   b) Realize the 2 input NAND gate by using pseudo NMOS logic. [L2][CO3][5M]
4. a) Explain dynamic CMOS logic circuit with any one example. [L1][CO3][5M]
   b) Mention its advantages & disadvantages? [L1][CO3][5M]
5. Write short notes on
   a) Domino CMOS logic. [L2][CO3][5M]
   b) NORA logic. [L2][CO3][5M]
6. a) Explain in detail about DCV logic. [L2][CO3][7M]
   b) Write notes on complex logic gates. [L1][CO3][3M]
7. What is the necessity of floor planning concept in VLSI circuits? and discuss with suitable example. [L3][CO3][10M]
8. What are the design methods used in physical design cycle? Explain the each term with suitable diagrams. [L3][CO3][10M]
9. a) Explain how the clock and power distributions employed in VLSI design circuits with diagrams. [L2][CO3][5M]
   b) Write about Power delay estimation in VLSI circuits. [L2][CO3][5M]
10. Write about the following
    a) Floorplanning [L2][CO3][4M]
    b) Placement [L2][CO3][3M]
    c) Routing [L2][CO3][3M]

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UNIT –IV

Subsystem Design

1. Explain the design of different adders in sub circuit design with neat sketches. [L3][CO4][5M]
2. a) What is shifter? List the types of shit registers. [L3][CO4][5M]
   b) Draw and explain the shifter implemented by using full adder. [L2][CO4][5M]
3. Write about the following sub circuits
   a) Parity generators [L2][CO4][5M]
   b) Comparators [L3][CO4][5M]
4. Design a Arithmetic and Logic Unit circuit with four functions by using multiplexer logic. [L4][CO4][10M]
5. a) Explain about different types of memory elements. [L3][CO4][5M]
   b) Realize the 4*4 array multiplier [L2][CO4][5M]
6. a) Explain the working of Zero/one detector implemented with adder circuit. [L2][CO4][7M]
   b) List the advantages of Zero/one detector. [L2][CO4][3M]
7. Write short notes on
   a) Unsigned magnitude comparator [L2][CO4][5M]
   b) Asynchronous Counters [L2][CO4][5M]
8. a) Draw and Explain the circuit diagram of 3-bit LFSR with example. [L3][CO4][5M]
   b) Draw and Explain the Johnson counter. [L3][CO4][5M]
9. a) Draw and Explain the circuit diagram of four bit Carry ripple adder. [L3][CO4][5M]
   b) Draw and Explain the the ripple counter. [L2][CO4][5M]
10. a) Explain about 4 transistor Dynamic memory cell. [L2][CO4][5M]
    b) Explain the 6 transistor Static memory cell. [L2][CO4][5M]

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UNIT –V

Semiconductor Integrated Circuit Design and CMOS Testing

1.a) Compare the PROM,PAL, PLA. [L3][CO5][5M]
b) Design the PAL Structure for the Boolean function Y= AB'C'+ABC+A'B'C'+A'BC. [L4][CO5][5M]
2.a) Draw and explain the architecture of FPGA. [L3][CO5][5M]
b) Discuss the merits of FPGA over other architectures. [L2][CO5][5M]
3.a) Discuss in details about CPLD structure and explain each block. [L3][CO5][5M]
b) What is global routing? Discuss the advantages. [L2][CO5][5M]
4. Design the logic diagram of PLA for the following. [L4][CO5][10M]
Y1=A'B'C'+ABC+A'B+ABC'
Y2=ABC+A'B'C+AC
Y3=A'BC'+AB'C+B'C'
5.a) Discuss in detail about standard cell design with suitable diagrams. [L3][CO5][5M]
b) Write short notes on [L2][CO5][5M]
i) I/O pads
ii) SPLD
iii) LUT
6.a) What is the need for testing? and explain about Fault simulation. [L3][CO5][5M]
b) Discuss what the necessity of testing VLSI circuits. [L2][CO5][5M]
7.a) Explain bout design strategies for testing. [L2][CO5][5M]
b) With neat sketches list the testing of various stages. [L3][CO5][5M]
8. Explain in detail about testing during the VLSI life cycle with neat sketches. [L3][CO5][5M]
9.a) What is testing? And explain any three test principles. [L3][CO5][5M]
b) What is controllability and observability? [L3][CO5][5M]
10.a)What is fault simulation? [L1][CO5][3M]
b) Explain the stuck at 1 and stuck 0 faults with suitable diagrams. [L3][CO5][7M]