SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : STLD(19EC0401) **Course & Branch**: B.Tech - ECE

Year & Sem: I-B.Tech & II-Sem

UNIT –I

Binary Systems, Boolean Algebra & Logic gates

1. Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent. **(10M)L1, CO.1**
2. Perform the following
   a) Subtraction by using 10's complement for the given 3456 - 245. **(5M)L3, CO.1**
   b) Subtraction by using 2's complement for the given 111001-1010. **(5M)L3, CO.1**
3. a) Convert the following to Decimal and then to Octal. (i) 423416 (ii) 100100112. **(5M)L1, CO.1**
   b) Convert the following to Decimal and then to Hexadecimal. (i) 12348 (ii) 110011112 **(5M)L1, CO.1**
4. Simplify the following Boolean expression:
   (a) F = (A+B)(A'+C)(B+C). **(5M)L3, CO.1**
   (b) F = A+B+C'+D(E+F) **(5M)L3, CO.1**
5. a) Obtain the truth table of the following Boolean function and express the function as sum of minterms and product of maxterms F = (A+B) (B+C) **(5M)L3, CO.1**
   b) Simplify the following Boolean functions to minimum number of literals **(5M)L3, CO.1**
   (i) xyz + x'y + xyz'. (ii) xz + x'yz.
6. Convert the following to Decimal and then to Octal **(10M)L1, CO.1**
   (a) 1234_{16} (b) $12EF_{16}$ (c) 10110011_2 (d) 10001111_2 (e) 352_{10}
   (f) 999_{10}
7. a) Simplify the following Boolean expressions to minimum no. of literals. **(5M)L3, CO.1**
   i. ABC+A'B+ABC' ii. (BC'+A'D)(AB'+CD')
   iii. x'yz+xz iv. xy+x(wz+wz')
   b) Obtain the Dual of the following Boolean expressions. **(5M)L3, CO.1**
   i. AB+A(B+C)+B'(B+D) ii. A+B+A'B'C
   iii. A'B+A'BC'+A'BCD+A'BC'D'E iv. ABEF+ABE'F'+A'B'EF
8. (a) State Duality theorem. List Boolean laws and their Duals. **(5M)L1, CO.1**
   (b) Simplify the following Boolean functions to minimum number of literals: **(5M)L3, CO.1**
   i. F = ABC + ABC' + A'B ii. F = (A+B)' (A'+B')
9. a) Convert the following to binary and then to gray code. **(5M)L1, CO.1**
   (i) $(1111)_{16}$ (ii) $(BC54)_{16}$ (iii) $(237)_8$ (iv) $(164)_{10}$ (v) $(323)_8$
   b) Perform the following using BCD arithmetic **(5M)L3, CO.1**
   (i) $(79)_{10} + (177)_{10}$ (ii) $(481)_{10} + (178)_{10}$
10. Convert the following to binary and then to gray code. **(10M)L1, CO.1**
    (a) $(1111)_{16}$ (b) $(BC54)_{16}$ (c) $(237)_8$ (d) $(164)_{10}$ (e) $(323)_8$

UNIT –II

Gate -Level Minimization

1. a) Minimize the following Boolean function using K-Map **(5M)L2, CO.1**
   F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).
   b) Realize it using NAND Gates. **(5M)L2, CO.1**
2. Minimize the given Boolean function F(A,B,C,D) = Σ m(0,1,2,3,6,7,13,15) using tabulation method and implement using basic gates **(10M)L2, CO.1**
3. a) Simplify the following Boolean expressions using K-map **(5M)L3, CO.1**
   F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z
   b) Implement the same using NAND gates. **(5M)L3, CO.1**
4. Simplifying the following expression using tabulation technique. **(10M)L3, CO.1**
   F=Σm(0,1,2,8,9,15,17,21,24,25,27,31)
5. a) Simplify the following expression using the K-map for the 3-variable. **(5M)L3, CO.1**
   Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
   b) Simplify the Boolean function F(A,B,C,D)=∑(1,3,7,11,15)+d(0,2,5) **(5M)L3, CO.1**
6. a) Implement the following Boolean function using NOR gates. **(5M)L3, CO.1**
   Y=(AB'+A'B)(C+D').
   b) Simplify the following Boolean function for minimal POS form using K-map
   F(X,Y,Z) = X'YZ + XY'Z' + XYZ + XYZ' **(5M)L3, CO.1**
7. Simplify the Boolean function by using tabulation method **(10M)L3, CO.1**
   F(a,b,c,d)=Σm(0,1,2,5,6,7,8,9,10,14)
8. Simplify the following Boolean function in POS form using K-map **(10M)L3, CO.1**
   F(A,B,C,D) = Σ(1,2,4,5,9,12,13,14)
9. Simplify the following Boolean function using Tabulation method **(10M)L3, CO.1**
   Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)
10. a) Write the advantages of Tabulation method over K-Map method. **(2M)L5, CO.1**
    b) Write the given Boolean expression f = A+B in Sum of minterms. **(2M)L5, CO.1**
    c) SOP of F(x, y, z)=Σ(2, 3, 6, 7). **(2M)L3, CO.1**
    d) Implement OR gate using only two input NAND gates **(2M)L3, CO.1**
    e) Implement the following Boolean equation using only NAND gates Y=AB+CDE+F. **(2M)L3, CO.1**

UNIT –III

Combinational Logic

1. a) Design & implement a 4-bit Binary-To-Gray code converter. **(5M)L1, L3 CO.2**
   b) Design a 4 bit binary-to-BCD code converter **(5M)L1, L3 CO.2**
2. a) Design & implement BCD to Excess-3 code converter. **(5M)L1, L3 CO.2**
   b) Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. **(5M)L1, L3 CO.2**
3. a) Design & implement Full Adder with truth table. **(5M)L1, L3 CO.2**
   b) Design & implement Full Subtractor with truth table. **(5M)L1, L3 CO.2**
4. Explain Carry Look Ahead Adder circuit with the help of logic diagram. **(10M)L2, CO.2**
5. Construct a BCD Adder-circuit. **(10M)L2, CO.2**
6. Implement 4-bit Magnitude Comparator and write down its design procedure. **(10M)L3, CO.2**
7. a) Design & implement Full Adder using Decoder. **(4M)L1,L3 CO.2**
   b) Implement a 2-bit Magnitude comparator and write down its design procedure. **(6M)L1,L3 CO.2**
8. What is encoder? Design octal to binary encoder. **(10M)L1, CO.2**
9. a) Implement the following Boolean function using 8:1 multiplexer. **(5M)L3, CO.2**

   $F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.$

   b) What is multiplexer? Construct 4*1 multiplexer with logic gates and truth table **(5M)L3, CO.2**
10. a) Draw the basic structure of combinational logic circuit **(2M)L3, CO.2**
    b) Design the full adder using half adders **(2M)L1, CO.2**
    c) Implement 2-bit by 2-bit multiplier with half adders **(2M)L3, CO.2**
    d) Realize a 2-bit comparator using gates **(2M)L3, CO.2**
    e) What is priority encoder? Mention its operation **(2M)L1, CO.2**

UNIT –IV

Synchronous Sequential Logic

1. a) Design D Flip Flop by using SR Flip Flop and draw the timing diagram. **(5M)L1, CO.2**
   b) Write the differences between combinational and sequential circuits. **(5M)L5, CO.2**
2. a) Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop. **(5M)L3, CO.2**
   b) Design T Flip Flop by using JK Flip Flop and draw the timing diagram. **(5M)L1, CO.2**
3. a) Draw the circuit of JK flip flop using NAND gates and explain its operation. **(5M)L3, CO.2**
   b) Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops. **(5M)L1, CO.2**
4. a) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram. **(5M)L1, CO.2**
   b) A clocked sequential circuit with single input x and single output z produces an output z=1 whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops. **(5M)L3, CO.2**
5. A sequential circuit with two D-flip flops A and B, two inputs ‘x’ and ‘y’ and one output ‘z’ is specified by the following next state and output equation. **(10M)L3, CO.2**

   $A(t+1) = x'y+xA$, $B(t+1) = x'B+xA$ and $Z = B$

   i) Draw the logic diagram of the circuit.
   ii) List the state table and draw the corresponding state diagram
6. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. **(10M)L1,L3, CO.2**
7. With a neat sketch explain MOD 6 Johnson counter using D FF. **IES 2015** **(10M)L3, CO.2**
8. Implement 6-bit ring counter using suitable shift register. Briefly describe its operation. **(10M)L3, CO.2**
9. Design a binary counter having repeated binary sequence using JK flip flops :0,1,2,4,5,6. **(10M)L1, CO.2**
10. a) Write the difference between Latch and Flip flop **(2M)L5, CO.2**
    b) List asynchronous inputs of a sequential device **(2M)L1, CO.2**
    c) Draw the block diagram of sequential circuit using combinational circuit and memory unit. **(2M)L3, CO.2**
    d) Draw the logic circuit of flip-flop and truth table using NOR gates. **(2M)L3, CO.2**
    e) Give the comparison between combinational circuits and sequential circuits. **(2M)L1, CO.2**

UNIT –V

Finite State Machines & Programmable Memories

1. Implement the following Boolean function using PLA **(10M)L3, CO.3**
   (i)F(w,x,y,z) = Σm(0,1,3,5,9,13) (ii)F(w,x,y,z)) = Σm(0,2,4,5,7,9,11,15)
2. Implement the following Boolean function usingPAL. **(10M)L3, CO.3**
   (i)A(w,x,y,z) = Σm(0,2,6,7,8,9,12,13) (ii)B(w,x,y,z)) = Σm(0,2,6,7,8,9,12,13,14)
   (iii)C(w,x,y,z) = Σm(1,3,4,6,10,12,13) (iv)D(w,x,y,z)) = Σm(1,3,4,6,9,12,14)
3. Implement the following Boolean function usingPLA **(10M)L3, CO.3**
   (i)F1= Σm(0,1,2,3,8,10,12,14) (ii)F2 = Σm(0,1,2,3,4,6,8,10,12,14).
4. Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7). **(5M)L3, CO.3**
5. Discuss Mealy & Moore Machine models of sequential machines. **(10M)L1, CO.2**
6. Explain the minimization procedure for determining the set of equivalent state of a specified machine M. **(10M)L2, CO.2**
7. Explain the following related to sequential circuits with suitable examples.
   a)State diagram **(2M)L1, CO.1**
   b) State table **(2M)L1, CO.1**
   c) State assignment **(6M)L1, CO.1**
8. a) Differentiate among ROM, PROM ,DROM ,EPROM, EEPROM, RAM. **(5M)L3, CO.3**
   b) Explain about memory decoding. **(5M)L3, CO.3**
9. Given the 8-bit data word 01011011,generate the 12-bit composite word for the hamming code that corrects and detects single errors. **(10M)L3, CO.3**
10. Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure. **(10M)L3, CO.3**

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QUESTION BANK (OBJECTIVE)

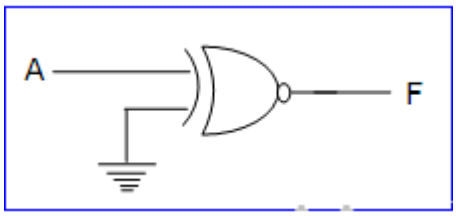
Subject with Code : STLD(19EC0401) **Course & Branch**: B.Tech - ECE

Year & Sem: I-B.Tech & II-Sem **Regulation:** R19

UNIT –I

Number System & Boolean Algebra

1. Indicate which of the following logic gates can be used to realized all possible combinational logic functions. **GATE 1989 [ ]**
   (A) OR gate **(B)**NAND gates only **(C)** EX-OR gate **(D)** NOR & NAND gates
2. Boolean expression for the output of XNOR logic gate with inputs A and B is **GATE 1993 [ ]**
   (A) AB' + A'B **(B)** (A(B)' + AB **(C)** (A' + (B)(A + B') **(D)** (A' + B')(A + (B)
3. The output of a logic gate is '1' when all its inputs are at logic '0'. The gate is either **GATE 1994 [ ]**
   (A) a NAND or an EX-OR gate **(B)**a NOT or an EX-NOR gate
   (C)an OR r an EX-NOR gate (D)an AND or an EX-OR gate
4. The output of the logic gate shown is **GATE 1997 [ ]**



(A) 0 **(B)** 1 **(C)** A **(D)** A'

5. 2's complement representation of a 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is **GATE 1993 [ ]**
   (A)0 **(B)** 1 **(C)** 32,767 (D) 65,535
6. Two 2's complement numbers having sign bits x and y are added and the sign bit of the result is z. Then, the occurrence of overflow is indicated by the Boolean function. **GATE 1998 [ ]**
   A) xyz (B) $\bar{x}\bar{y}\bar{z}$ (C) $\bar{x}\bar{y}z + xy\bar{z}$ (D) xy + yz + zx
7. 4 – bit 2's complement representation of a decimal number is 1000. The number is **GATE 2002 [ ]**
   (A) +8 **(B)** 0 **(C)** -7 **(D)** -8
8. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is _____. **GATE 2014 [ ]**
   (A) 4 **(B)** 3 **(C)**2 **(D)** 8

9. The two numbers represented in signed 2's compliment form are P = 11101101 and Q = 11100110. If Q is subtracted from P, the value obtained in signed 2's compliment form is___. **GATE 2008 [ ]**

(A) 100000111 **(B)** 00000111 **(C)** 11111001 (D) 111111001

10. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this number system, the BCP code 100010011001 corresponds to the following number in base-5 system. **GATE 2001 [ ]**

(A) 423 **(B)** 1324 **(C)** 2201 **(D)** 4231

11. Boolean expression for the output of XNOR logic gate with inputs A and B is **GATE 1993 [ ]**

(A) AB' + A'B **(B)** (A(B)' + AB **(C)**(A' + (B)(A + B') **(D)** (A' + B')(A + (B)

12. The 2's complement representation of – 17 is **GATE 2001 [ ]**

(A) 01110 **(B)**101111 **(C)** 11110 **(D)**10001

13. The range of signed decimal numbers that can be represented by 6 bit 1's complement form is **GATE 2004 [ ]**

(A) -31 to +31 **(B)** -63 to +64 **(C)** -64 to +63 **(D)**-32 to +31

14. Decimal 43 in Hexadecimal and BCD number system is respectively. **GATE 2005 [ ]**

(A) B2, 0100 0011 **(B)** 2B, 0100 0011 **(C)** 2B, 0011 0100 **(D)** B2, 0100 0100

15. X = 01110 and Y = 11001 are two 5 bit binary numbers represented in 2's compliement format. The sum of X and Y represented in 2's compliment format using 6 bits is **GATE 2004 [ ]**

(A) 100111 **(B)** 001000 **(C)** 000111 **(D)** 101001

16. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is ___. **GATE 2014 [ ]**

(A) 1 **(B)** 2 **(C)** 4 **(D)** 8

17. The Boolean function A + BC is a reduced form of **GATE 1997 [ ]**

(A) AB + BC **(B)** (A + (B)(A + (C) **(C)** A'B + AB'C **(D)** (A + (C)B

18. The logical expression Y = A + A'B is equivalent to **GATE 1999 [ ]**

(A) AB **(B)** A'B **(C)** A' + B **(D)** A + B

19. The minimized form of the logical expression $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C}$ is **GATE 1999 [ ]**

(A) $\bar{A}\bar{C} + B\bar{C} + \bar{A}B$ **(B)** $A\bar{C} + C\bar{B} + \bar{A}B$ **(C)** $C\bar{A} + C\bar{B} + \bar{A}B$ **(D)** None

20. The Boolean expression AC + BC' is equivalent to___ **GATE 2004 [ ]**

(A) $\bar{A}C + B\bar{C} + \bar{A}C$ **(B)** $B\bar{C} + AC + B\bar{C} + \bar{A}C\bar{B}$

(C) $AC + B\bar{C} + \bar{B}C + \bar{A}BC$ **(D)** $ABC + \bar{A}B\bar{C} + AB\bar{C} + AB\bar{C}$

21. The following Boolean expression Y = A'B'C'D + A'BCD' + AB'C'D + ABC'D' can be minimized to **GATE 2007 [ ]**

(A) $\bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C} + A\bar{C}D$ **(B)** $\bar{A}\bar{B}\bar{C}D + BC\bar{D} + A\bar{B}\bar{C}D$

(C) $\bar{A}BC\bar{D} + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$ **(D)** None

22. The number of Boolean functions that can be generated by n variables is equal to **GATE 1990 [ ]**

(A) $2^{2^{n-1}}$ **(B)** 2^{2^n} **(C)** 2^{n-1} **(D)** 2^n

23. The hexadecimal representation of 756_8 is _____. **[ ]**

(A). $1EE_H$ **(B).** 178_H **(C).**$EE1_H$ **(D).** 436_H

24. A group of 16 bits is known as ____ **[ ]**
(A). Bit (B). Byte (C). Word (D). Nibble

25. A 15-bit hamming code requires _____. [ ]
(A). 4 parity bits (B). 5 parity bits (C).10 parity bits (D).7 parity bits

26. Applying Canonical theorem to the expression, $\overline{A+B+C+D}$, we get ____. **[ ]**
(A).$\overline{A}\overline{B}\overline{C}\overline{D}$ (B).$\overline{A}+\overline{B}+\overline{C}+\overline{D}$ (C). $A+\overline{B}+\overline{C}+D$ (D). $\overline{A}+B+C+\overline{D}$

27. Convert binary 101011110010 to hexadecimal. [ ]
(A). $9E2_{16}$ (B). $AF2_{16}$ (C). $9FE_{16}$ (D). $FD2_{16}$

28. The BCD number for decimal 447 is ____. [ ]
(A).1100 1011 1000 (B).0100 0100 0011 (C).0101 0100 0011(D).0100 0100 0111

29. Hexadecimal number E is equal to octal number [ ]
(A). 15 (B). 16 (C). 17 (D). 18

30. Which of the following gates is known as coincidence gate? [ ]
(A). AND (B). OR (C). NAND (D) EX-NOR

31. Hexadecimal letters A through F are used for decimal equivalent values from___. [ ]
(A). 1 through 6 (B). 9 through 15 (C). 10 through 15 (D). 11 through 16

32. The number of distinct Boolean expressions of 4 variables is **GATE 2003** [ ]
(A). 16 (B). 256 (C). 1024 (D). 65536

33. Excess-3 code is a ____code. [ ]
(A). Weighted (B). cyclic(C). Error correcting (D). Self-complementing

34. Which of the following code is referred as unit distance code? [ ]
(A). Excess-3 code (B). BCD code (C). Gray code (D). ASCII code

35. Which of the following is error correcting code? [ ]
(A). EBCDIC (B). GRAY (C). Hamming (D). ASCII

36. The operation A $\oplus$ B represents ____ [ ]
(A). A-B (B).$\overline{A}B+A\overline{B}$ (C). AB+$\overline{A}\overline{B}$ (D). A - $\overline{B}$

37. When $\overline{A}, \overline{B}$ are the inputs to a NAND gate, according to De Morgan's theorem, the output expression could be [ ]
(A). X=A+B (B). X=$\overline{AB}$ (C). AB (D). X=A$\overline{B}$

38. The minimum number of NAND gates required to implement the Boolean function A + AB' + AB'C is equal to **GATE 1995** [ ]
(A) Zero **(B)** 1 **(C)** 4 **(D)** 7

39. The subtraction of a binary number Y from another binary number X, done by adding 2's compliment of Y to X, results in a binary number without overflow. This implies that the result is **GATE 1987** [ ]
(A) Negative and is in normal form **(B)** Negative an is in 2's compliment form
(C) Positive and is in normal form **(D)** Positive and is in 2's compliment form

40. 2's complement representation of a 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is **GATE 1993** [ ]
(A) 0 **(B)** 1 **(C)** 32,767 **(D)** 65,535

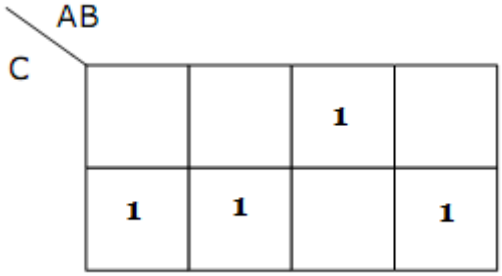
UNIT-II
Gate Level Minimization

1. The number of product terms in the minimized sum of product expression obtained through the following K-map (where "d" denotes don't care states) **GATE 2006 [ ]**

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

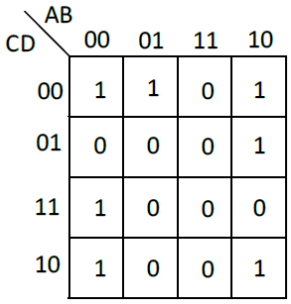
A). 2 **B).** 3 **C.** 4 **D.** 5

2. A Boolean function, F is given as sum of product (SOP) terms as P = ∑m (3, 4, 5, 6) with A, B and C as inputs. The function, F can be expressed on the karnaugh's map shown below. What will be the minimized SOP expression for F **GATE 1994 [ ]**



A. $\overline{A}BC + A\overline{B} + A\overline{C}$ **B.** $\overline{A}\overline{B}C + A\overline{B} + A\overline{C}$ **C.** $\overline{A}BC + \overline{A}\overline{B} + A\overline{C}$ **D.** None

3. The K-map for a Boolean function is shown in figure. The number of essential prime implicants for this function is **GATE 1998 [ ]**



A). 6 **B).** 5 **C.** 4 **D.** 8

4. In the sum of products function f(X,Y,Z) =Σ(2,3,4,5), the prime implicates are **GATE 2012 [ ]**

A. $\overline{X}\overline{Y}, X\overline{Y}$ **B.** $\overline{X}\overline{Y}, X\overline{Y}Z$ **C.** $\overline{X}\overline{Y}\overline{Z}, X\overline{Y}$ **D.** $\overline{X}\overline{Y}\overline{Z}, X\overline{Y}, XYZ$

5. When grouping cells within a K-map, the cells must be combined in groups of____.**[ ]**
(A).1,2,3,4,etc (B). 1,2,4,8, etc, (C). 1,3,5,7 (D). 1,10,20

6. The adjacent cells/squares of minterm 5 in a 4 – variable K-map is **[ ]**
(A). 1,4,7,13 (B). 0,1,3,2 (C). 8,9,10,11 (D). 12,13,4,7

7. Sum of all max terms is **[ ]**
(A). 1 (B). 0 (C). 1 or 0 (D). None

8. A K-map with 4 variables has _____ min/max terms [ ]
   (A). 2 (B). 4 (C). 8 (D). 16
9. The complement of min term 4 is [ ]
   (A). min term 4 (B). min term 5 (C). max term 4 (D). max term 5
10. A n variable K-map can have [ ]
   A. n^2 cells **B.** 2^n cells **C.** n^n cells **D.** n^{2n} cells
11. Each term in the standard SOP form is called a _____. [ ]
   A. minterm **B.** maxterm **C.** Don't care **D.** literal
12. The binary no. destinations of the rows and columns of the K-map are in [ ]
   A. Binary Code **B.** BCD code **C.** Gray Code **D.** XS-3 code
13. The no. of cells in a 6 variable K-map is [ ]
   A. 6 **B.** 12 **C.** 36 **D.** 64
14. An 8-square is called ____ [ ]
   A. a pair **B.**A quad **C.** an octet **D.** a cube
15. The NOR-NOR realization is equivalent to ___ [ ]
   A. AND-OR realization **B.** NOT-AND realization
   C. OR-NOT realization **D.** OR-AND realization
16. A 16 square eliminates [ ]
   A.2 Variables **B.** 3 variables **C.** 4 variables **D.**None
17. In the Quine - McClusky method of minimization of the function f(A,B,C,D) the PI corresponding to _11_ is [ ]
   A. $\overline{A}BC\overline{D}$ **B.** BC **C.** $\overline{B}\overline{C}$ **D.** $A\overline{B}\overline{C}D$
18. The code used for labelling the cells of a K-map is [ ]
   A. 8-4-2-1 binary **B.** Hexadecimal **C.** Gray **D.** Octal
19. The total number of 1s present in minterm is called a [ ]
   A. Index **B.** Weight **C.** Logic level **D.** term number
20. An 8-squares eliminates [ ]
   A. 2 variables **B.** 3 variables **C.** 4 variables **D.** 8 variables
21. An 2-square is called ____ [ ]
   A. a pair **B.** A quad **C.** an octet **D.** a cube
22. An 4-square is called ____ [ ]
   A. a pair **B.**A quad **C.** an octet **D.** a cube
21. An 16-squares eliminates [ ]
   A. 2 variables **B.** 3 variables **C.** 4 variables **D.** 8 variables
23. The terms which cannot be combined further in the tabular method are called __ [ ]
   A. Canonical **B.** Prime Implicants **C.** variables **D.**None
24. The reduced SOP for the expression f(A,B,C)=Σm(0,1,5)+Σd(4,7) is [ ]
   A. AB **B.** BC **C.** $\overline{B}$ **D.** ABC
25. A 2 square eliminates [ ]
   A.1 Variables **B.** 3 variables **C.** 4 variables **D.**None
26. A 4 square eliminates [ ]
   A.2 Variables **B.** 3 variables **C.** 4 variables **D.**None
27. F(X,Y,Z)=XY+XZ, Convert the same in to simplest POS form [ ]

A. $(\overline{X+Y})(\overline{X+Z})$ **B.** $(\overline{X+Y})+(\overline{X+Z})$ **C.** $(\overline{X}\,\overline{Y})(\overline{X}\,\overline{Z})$ **D.** None

28. $\overline{A}B+A\overline{B}=$ [ ]
A. $A\oplus B$ **B.** $A\Theta B$ **C.** $A\oplus AB$ **D.** None

29. $\overline{A}\,\overline{B}+AB=$ [ ]
A. $A\oplus B$ **B.** $A\Theta B$ **C.** $A\oplus AB$ **D.** None

30. The expression f=(A+B)($\overline{A}+B)(\overline{A}+\overline{B})$) in terms of Maxterms is [ ]
A. ΠM(0,1,3) **B.** Σm(0,1,3) **C.** ΠM(0,2,3) **D.** Σm(0,2,3)

31. Realize the function F=Σm(0,1,2,3) using K-map [ ]
A.AB **B.** 1 **C.**A **D.**None

32. A 4 variable K-map can have _____ squares. [ ]
A.4 **B.** 8 **C.** 16 **D.** 32

33. A 5 variable K-map can have _____ squares. [ ]
A.4 **B.** 8 **C.** 16 **D.** 32

34. A real minimal expression is the minimal of _____ expressions. [ ]
A.SOP **B.** POS **C.**Both **D.**None

35. Each term in the standard POS form is called a _____. [ ]
B. minterm **B.** maxterm **C.** Don't care **D.** literal

36. Realize the function F=ΠM(0,1,2,3) using K-map [ ]
A.AB **B.** 1 **C.**A **D.**None

37. Realize the function F=ΠM(0,1,3) using K-map [ ]
` **A.** $A\overline{B}$ **B.** 1 **C.** $\overline{A}+B$ **D.**None

38. Realize the function F=ΣM(0,1,3) using K-map [ ]
A. $\overline{A}+B$ **B.** 1 **C.** $A\overline{B}$ **D.** None

39. Realize the function F=ΣM(1,2) using K-map [ ]
A. $\overline{A}B+A\overline{B}$ **B.** $\overline{A}B$ **C.** $A\overline{B}+A\overline{B}$ **D.** None

40. Realize the function F=ΣM(0,1,2) using K-map [ ]
A. $\overline{A}B+A\overline{B}$ **B.** $\overline{A}B$ **C.** $\overline{B}+\overline{A}$ **D.** None

41. For an n – variable Boolean function, the maximum number of prime implicants are [ ]
A.2(n – 1) **B.** n/2 **C.** 2^n **D.** $2^{(n-1)}$

UNIT-III
Combinational Logic Circuits

1. The combinational circuits are_____ than sequential circuits [ ]
A) slower **B)** faster **C)** same speed **D)** None
2. In combinational circuits the o/p depends on _____i/p [ ]
A) present **B)** past **C)** A & B **D)** None
3. Full adder circuit adds _____number of bits at a time [ ]
A) 5 **B)** 2 **C)** 5 **D)** 3
4. Half adder circuit adds _____number of bits at a time [ ]

A) 5 **B)** 2 **C)** 5 **D)** 3

5. Serial binary adder is a _____circuit [ ]
   A) combinational **B)** sequential **C)** A or B **D)** None
6. A 4 bit parallel adder is designed using _____number of full adders [ ]
   A) 2 **B)** 4 **C)** 5 **D)** 3
7. The logic expression for carry of half adder circuit is_____ [ ]
   A) A'B **B)** AB **C)** AB' **D)** None
8. The logic expression for sum of half adder circuit is_____ [ ]
   A) A'B **B)** A xor B **C)** AB' **D)** None
9. In a half subtractor circuit borrow expression is_____ [ ]
   A) A'B **B)** AB **C)** AB' **D)** None
10. The logic expression for difference of half subtractor circuit is_____ [ ]
    A) A xor B xor C **B)** B xor C **C)** A xor B **D)** None
11. The logic expression for sum of full adder circuit is_____ [ ]
    A) A'BC **B)** A xor B xor C **C)** B xor C **D)** None
12. The logic expression for carry of full adder circuit is_____ [ ]
    A) ABC **B)** A xor B xor C **C)** B xor C **D)** None
13. In a full subtractor circuit difference expression is_____ [ ]
    A) A xor B xor C **B)** B xor C **C)** A xor C **D)** B xor C
14. In a full subtractor circuit borrow expression is_____ [ ]
    A) A xor B xor C **B)** B xor C **C)** A xor C **D)** None
15. The full adder circuit is implemented using _____number of half adder circuits [ ]
    A) 3 **B)** 1 **C)** 2 **D)** 4
16. The full subtractor circuit is implemented using _____number of half subtractor circuit [ ]
    A) 3 **B)** 1 **C)** 2 **D)** 4
17. Complement of a bit in adder - subtractor circuit is [ ]
    A) inverter **B)** XOR **C)** AND **D)**None
18. Carry look ahead adder reduces _____ [ ]
    A) carry propagation time **B)** carry generation time **C)** sum generation time **D)** None
19. For an n-bit adder there are _____ gate levels for the carry to propagate from input to output [ ]
    A)3n **B)** 4n **C)** 2n **D)** None
20. In carry look ahead adder C_{i+1}=_____ [ ]
    A)$G_i+P_iC_i$ **B)** $G_i+P_{i+1}C_i$ **C)** $G_{i+1}+P_iC_i$ **D)**None
21. In magnitude comparison of A,B the output of a xor gate if they are equal is [ ]
    A)1 **B)**0 **C)** high impedance state **D)** None
22. In magnitude comparison of A,B the output of a xnor gate if they are equal is [ ]
    A)1 **B)**0 **C)** high impedance state **D)** None
23. In magnitude comparison of A,B the output of a xor gate if they are unequal is [ ]
    A)1 **B)**0 **C)** high impedance state **D)** None
24. In magnitude comparison of A,B the output of a xnor gate if they are unequal is [ ]
    A)1 **B)**0 **C)** high impedance state **D)** None
25. Minimum number of half adders required for 2 bit multiplier is [ ]

A)2 **B)**3 **C)**4 **D)** None

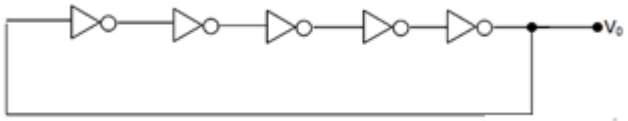
26. If A=1010 and B=0100 .Then output of a 4 bit parallel adder is_____ [ ]
A) 1011 **B)** 1100 **C)** 1110 **D)** None
27. A decoderwith n input provides _____minterms at the output. [ ]
A)n **B)** 2n **C)** 2^n **D)** None
28. A encoder has --------number of inputs and --------number of outputs [ ]
A)n& 2n **B)** 2n & n **C)** 2^n & n **D)** None
29. The number of output lines in 1X4 demultiplexer is_____ [ ]
A)3 **B)** 8 **C)** 1 **D)** 4
30. The number of AND gates required to implement 3 X 8 decoder along with 3 not gates is___ [ ]
A)5 **B)** 7 **C)** 8 **D)** None
31. To implement full adder ---------size decoder is required [ ]
A) 2x4 **B)** 3x8 **C)** 4x2 **D)** None
32. A 4X16 decoder can be designed using _____ number of 3x8 decoders [ ]
A) 2 **B)** 3 **C)** 4 **D)** 8
33. An octal to binary encoder is implemented using 3_____ gates [ ]
A) AND **B)** NAND **C)** XOR **D)** None
34. The number of select inputs in 32X1 multiplexer is_____ [ ]
A)5 **B)** 6 **C)** 4 **D)**None
35. The binary variable (A=**B)** is equal to _____ only if all pairs of digits of the two numbers are equal [ ]
A)0 **B)**1 **C)** X **D)** None
36. In a 4X2 priority encoder with D3 with highest priority the output XY for input 1111 is_____ [ ]
A)00 **B)**11 **C)** 10 **D)**None
37. The decimal adder is also known as _____adder [ ]
A) Ripple carry **B)** excess 3 **C)**BCD **D)** carry look ahead
38. Multiplexer is also called as [ ]
A)Data Distributer **B)** Data Selector **C)** Data Analyser **D)** None
39. Demultiplexer is also called as [ ]
A)data distributer **B)** data selector **C)** data analyzer **D)** None
40. The decimal adder is also known as _____adder [ ]
A)Ripple carry **B)** excess 3 **C)**BCD **D)** carry look ahead
41. The number of 4X1 multiplexers required to design 16X1 multiplexer is _____ [ ]
A) 5 **B)** 6 **C)** 4 **D)** None
42. A 2bit multiplier can design using minimum of [ ]
A) 2 AND gates only **B)** 2XOR & 4 AND **C)** 2 NOR& XNOR **D)** None

UNIT-IV
Sequential Logic Circuits

1. The output Y of a 2-bit comparator is logic 1 whenever the 2 bit input A is greater than the 2 bit input B. The number of combinations for which the output is logic 1, is
A. 4 **B**. 6 **C**. 8 **D**. 10
GATE 2012 [ ]
2. A switch-tail ring counter is made by using a single D flip flop. The resulting circuit is a
GATE 1995 [ ]
A. SR flip flop **B**. JK flip flop **C**. D flip flop **D**. T flip flop

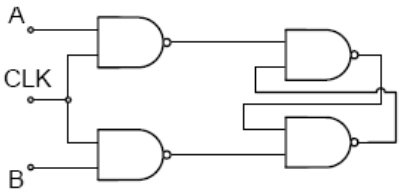
3. An SR latch is a **GATE 1995** [ ]
   A. Combinational circuit **B**. Synchronous sequential circuit
   C. One bit memory element **D**. One clock delay element
4. The present output Q_n of an edge triggered JK flip-flop is logic '0'. If j = 1, then Q_{n+1} is **GATE 2005** [ ]
   A. Cannot be determined **B**. Will be logic '0'
   C. Will be logic '1' **D**. Will race around
5. A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 nsec, the maximum clock frequency that can be used is equal to ____. **GATE 1990** [ ]
   A. 20 MHz **B**. 10 MHz **C**. 5 MHz **D**. 4 MHz
6. Synchronous counters are _____ than the ripple counters. **GATE1994** [ ]
   A. Slower **B**. Faster **C**. Moderate **D**. None
7. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then **GATE 2003** [ ]
   A. R = 10 ns, S = 40 ns **B**. R = 40 ns, S = 10 ns
   C. R = 10 ns, S = 30 ns **D**. R = 30 ns, S = 10 ns
8. In sequential Circuits, the output variable depends on _____of the input variable. [ ]
   A. Present State **B**. Past State **C**. Both **D**. None
9. The Serial adder is a _____Circuit. [ ]
   A. Combinational **B**. Sequential **C**. Both **D**. None
10. The outputs of any sequential circuit are always _____to each other.
    A. Complementary **B**. Independent **C**. Pearson **D**. None
11. In S-R latch, if S=R=1, the present state of the latch is. [ ]
    A. 1 **B**. 0 **C**. Undetermined **D**. None
12. The D- latch sometimes called as _____ Latch. [ ]
    A. Flipflop **B**. Buffer **C**. Transparent **D**. None
13. _____and_____are building blocks of Sequential Circuits. [ ]
    A. Flipflop **B**. Latches **C**. Both **D**. None
14. In _____Triggering, the output of Flipflop responds to the input changes only when its enable input is Low. [ ]
    A. Negative Level **B**. Positive Level **C**. Edge **D**. None
15. If S=0, R=1 and CP = 0 to which Q_n= 0\1, the S-R Flipflop will be in __State. [ ]
    A. No change **B**. 1 **C**. 0 **D**. Undetermined
16. The Basic building block of D- flipflop is ____Flipflop. [ ]
    A. J-K **B**. Master-Slave **C**. S-R **D**. None
17. The output $Q_{n+1}$is delayed by one clock period for an D- Flipflop to which it is called as ____Flipflop. [ ]
    A. J-K **B**. Master-Slave **C**.S-R **D**. Delay
18. For the Inputs J=0, K=0, the output Q will be in ____state. [ ]
    A. Reset **B**. Undertermined **C**.Nochange **D**. Delay
19. In JK flipflop, when J = K = 1, the output the Flipflop will be in ____state. [ ]
    A. Reset **B**. Undertermined **C**. Toggling **D**. Delay
20. _____will not be an clock input of the Master-slave Flipflop. [ ]
    A. Edge Triggered **B**. Level Triggered **C**.Both **D**. None
21. The ____ Flipflop is a modification of JK Flipflop. [ ]
    A. J-K **B**. Master-Slave **C**.S-R **D**. T
22. If P = C = 0, the flipflop will be in _____ State. [ ]
    A. Reset **B**. Uncertan **C**.Nochange **D**. Delay

23. For Moore Sequential Circuit, the output depends on____ State. [ ]
A. Reset **B**. Present **C**.Previous **D**. Delay
24. The state reduction technique avoids _____states. [ ]
A. Reset **B**. Present **C**.Previous **D**. Redundant
25. The Input and Output of a register can be controlled by connecting ____. [ ]
A. Buffer **B**. Flipflop **C**. Tristate Buffers **D**. None
26. The _____ are used to transfer and storage of data in the registers. [ ]
A. Barrel Registers **B**. Shift Registers **C**. Tristate Buffers **D**. None
27. The acronym of SIPO is_____. [ ]
A. Serial In Parallel Out **B**. Serial In Page Out
C.SeriesIn Parallel Out **D**. None
28. The _____ register has capability of both shifts and parallel load. [ ]
A. Barrel Registers **B**. Universal Shift Registers **C**. Tristate Buffers **D**. None
29. The_____counters are simple in construction for more no. of states. [ ]
A. Synchronous **B**. Asynchronous **C**. Both **D**. None
30. The Major limitation of Ripple counter is_____. [ ]
A. Glitch Problem **B**. Asynchronous **C**. Both **D**. None
31. For **n** no. of Flipflops, the counter has ____no. of states. [ ]
A. n **B**. 2n **C**. 2^n **D**. None
32. The twisted counter is also called as _____Counter. [ ]
A. Ring **B**. Johnson **C**. Road **D**. None
33. The _____ Counter requires only half the no. of Flipflops compared to Standard counter. [ ]
A. Ring **B**. Johnson **C**. J-K **D**. None
34. For a counter of five-bit sequence, there are ____ states. [ ]
A. 10 **B**. 8 **C**. 4 **D**. 2
35. If all the Fliflops are triggered at the same time in an counter, then the counter is referred to as _____ Counter. [ ]
A. Synchronous **B**. Asynchronous **C**. Both **D**. None
36. An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter is approximately. [ ]
A. 1MHz **B**. 500 MHz **C**. 4 MHz **D**. 2 MHz
37. The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions [ ]
A. By applying J = 0, K = 0 and using a clock
B. By applying J = 1, K = 0 and using the clock
C. By applying J = 1, K = 1 and using the clock
D. By applying a synchronous preset input
38. Two D flip-flops are connected as a synchronous counter that goes through the following Q_B Q_A sequence 00 -> 11 -> 01 -> 10 -> 00-> ……. The connections of the inputs D_A and D_B are **GATE 2011** [ ]
A. $D_A = Q_B$, $D_B = Q_A$ **B.** $D_A = Q_B^1$, $D_B = Q_A^1$
C. $D_A = Q_A Q_B + Q_A^1 Q_B^1$, $D_B = Q_B^1$ **D**.None
39. For the ring oscillator shown in teh figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output?
GATE 2001 [ ]



A.10 MHz **B**. 100 MHz **C**. 1 GHz **D**. 2 GHz

40. Consider the given circuit. In the circuit, the race around **GATE 2012** **[ ]**
    A. does not occur
    B. Occur when CLK=0
    C. Occur when CLK=1, and A=B=1
    D. Occur when CLK=1, and A=B=0



UNIT –V
Programmable Devices

1. A 32X8 ROM consists of 32 words of _____bits each [ ]
   A) 4 **B**). 8 **C**). 16 **D**). None
2. The programmable logic devices are_____ [ ]
   A)ROM **B)** PLA **C)**. a and b **D)**. None
3. In PLA number of product terms is equal to number of _____gates [ ]
   A)OR **B)**. NAND **C)**. AND **D)**. None
4. In PLA number of product terms is equal to number of _____gates [ ]
   A). OR **B)** NAND **C)** AND **D)** None
5. In PAL AND gates are_____ [ ]
   A) Programmable **B)** fixed **C)** a and b **D)** None
6. In PAL OR gates are_____ [ ]
   A) Programmable **B)** fixed **C)** a and b **D)** None
7. In PROM AND gates are_____ [ ]
   A) Programmable **B)** fixed **C)** a and b **D)** None
8. In PROM OR gates are_____ [ ]
   A) Programmable **B)** fixed **C)** a and b **D)** None
9. In PLA AND gates are_____ [ ]
   A) Programmable **B)** fixed **C)** a and b **D)** None
10. In PLA OR gates are_____ [ ]
    A) Programmable **B)** fixed **C)** a and b **D)** None
11. Expansion of RAM [ ]
    A) read only memory **B)** random access memory **C)** A and B **D)** None
12. Expansion of FPGA [ ]
    A) field programmable gate array **B)** final programmable gate array
    C) field programmable gate array **D)** None
13. Expansion of CLB [ ]
    A) Configurable Logic Block **B)** Common Logic Block
    C) Control Logic Block **D)** None
14. Expansion of ROM [ ]
    A) read only memory **B)** random access memory **C)** a and b **D)** None
15. Expansion of PROM [ ]
    A) read only memory **B)** random access memory
    C) Programmable read only memory **D)** None

16. Expansion of EPROM [ ]
A) read only memory **B)** programmable read only memory
C) Erasable programmable read only memory **D)** None
17. Expansion of EEPROM [ ]
A) Read Only Memory **B)** Programmable Read Only Memory
C) Erasable Programmable Read Only Memory **D)** None
18. Refreshing is necessary in which memory cells [ ]
A) Static RAM **B)** Dynamic RAM **C)** EPROM **D)**None
19. DRAM is designed using_____ as a memory element [ ]
A) capacitor **B)** inductor **C)** flip-flops **D)**None
20. In compare to SRAM , DRAM has [ ]
A) more density **B)** less density **C)** equal density **D)**None
21. The cost/bit of DRAM storage is_____than SRAM [ ]
A) more **B)** less **C)** equal density **D)**None
22. Basic memory cell in SRAM [ ]
A) capacitor **B)** inductor **C)** flip-flops **D)**None
23. In EEPROM the programmed connections are erased with_____ [ ]
A) ultraviolet light **B)** electrical signal **C)** a or b **D)** None
24. In EPROM the programmed connections are erased with_____ [ ]
A) ultraviolet light **B)** electrical signal **C)** a or b **D)** None
25. A memory unit 64x8 has _____number of data lines [ ]
A) 4 **B)** 7 **C)** 10 **D)** None
26. The number of product terms in a PLA program table is 4.Then number of OR gates required is__ [ ]
A) 4 **B)** 5 **C)** 6 **D)** None
27. The number of product terms in a PAL program table is 12.Then number of AND gates required in design is__ [ ]
A) 8 **B)** 12 **C)** 6 **D)** None
28. For very high speed applications_____memory is used [ ]
A) RAM **B)** ROM **C)** CCD **D)**CAM
29. CAM can be accessed with the help of_____content [ ]
A). address **B)** data **C)** control **D)** None
30. Basically programmable devices are _____types [ ]
A) 2 **B)** 4 **C)** 3 **D)** 5
31. The sequential circuit in which the output depends only on the present state of the flip-flop is called a_____ [ ]
A)Mealy **B)** Moore **C)** Both **D)** None
32. A state which has no outgoing arcs is called a _____ state. [ ]
A) Edge **B)** End **C)** Terminal **D)** None
33. Each vertex in the subgraph belongs to _____state [ ]
A) One **B)** Two **C)** Three **D) None**
34. A table which consists ot the states of a minimal state machine is called a_ [ ]
A) Minimal cover table b. Maximal cover table c. Both d.None

Prepared by: